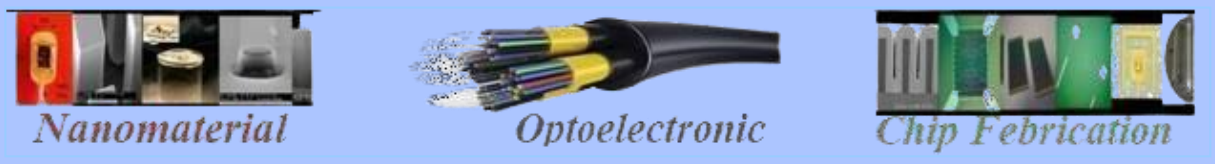
Abstract Proceeding of

Micro2023

10th International Conference on

Microelectronics, Circuits & Systems

01st and 03rd of July, 2023



Organizer:

Applied Computer Technology

Kolkata, West Bengal, India.

www.actsoft.org

In Association with:

International Association of Science, Technology and Management

ACT MICRO CCSN ESDA

Abstract Proceedings of

Micro2023

10th International Conference on

Microelectronics, Circuits & Systems

01st to 03rd of July, 2023

Organizer:

Applied Computer Technology
Kolkata, West Bengal, India.

www.actsoft.org

In Association with:

International Association of Science, Technology and Management

ACT

MICRO

CCSN

ESDA

Micro2023

10th international conference on

Microelectronics, Circuits and Systems

July 01st 2023	July 02nd and 03rd 2023
Venue: Hotel Vivanta Guwahati, Offline conference Link of conference: meet.google.com/uwc-tctf-wnc	Venue: Online conference Link of conference: meet.google.com/uwc-tctf-wnc

Proceedings Book with abstract of papers

Published dates: 01st July 2023

Published by: Dulal Acharjee, Director, Applied Computer Technology,

53 Teachers' Colony, Agarpara, Kolkata-700109, India.

Inaugural Song:

Prayer
Translated in English
By
Hillol Ray
http://www.iwvpa.net/rayh
http://www.iwvpa.net/rayh/index-hra.php
Desires are all yours,
You are the universal star-
You do your own works, mom,
People say, I do them from a far!!

You stuck elephant into clay,
And push a handicap to ascend hill-
To some, you offer "Brahmo" feet,
And make others descend downhill!!

I am a machine, you are the machinist,
I am the home; you are the homemaker-

I am the chariot, you are the charioteer,
You drive as you like, and I am a happy taker!!

"Milestone"
June 25, 2019
Garland, Texas, USA

Editorial

On behalf of the Applied Computer Technology, Kolkata, and International Association of Science, Technology and Management, the organizing committee of Micro2023 is delighted to invite you to the 10th international conference on Microelectronics, Circuits & Systems. The conference will be held as mixed mode, on 01st July at Hotel Vivanta, Guwahati, Assam, India, 02nd and 03rd July as Online mode. Micro2023 has been envisioned as physical mode on 01st July 2023. This conference with physical and virtual formats will provide an opportunity for our community to present their research works and collaborate with their peers across the Globe.

About 110 papers are received and 70 are selected for presentation. Most of the papers are in the areas of Microelectronics, Circuits and Systems Technology, MEMS, design and circuits, soft computing and optimization techniques, memory and storage circuits and devices, Nano-structures and Nanomaterials, Silicon and III-V Technology, CMOS scaling Issues, Sensor and IoT Networks, Analog/ RF and digital Circuits, VLSI, Power Electronics, Solid-state lighting, Optical Switch, Bio and Medical Electronics, Antenna Design etc.

Some good papers will be invited to forward to a special issue of the Journal of Microsystem Technologies of Springer-Nature, SCI indexed and having impact factor=2.5. Some other papers will be invited for inclusion to the Proceedings of LNEE (Lecture Notes on Electrical Engineering) book series of Springer having SCOPUS index and impact factor=0.6.

With due thanks and best wishes to all our team members including the Chief Guest, Keynote Speakers, invited speakers, chair persons, authors, participants etc. for sparing their valuable time in making the event a success in this typical pandemic period.

These abstract proceedings are prepared with the abstracts of all papers for the delegates of the conference and for listing the abstracts only either in offline/online. As most of the revised and extended versions of the papers will go for either SCIE Journal or Scopus indexed Book chapters. We have not given any ISBN number to this book as because, these papers will go for further online publications.

The Editors
Micro2023

Program Schedule of Micro2023

The Program Schedule: (Indian Standard Date/Time)

Date: 01/07/2023(dd/mm/yyyy): Venue: Hotel Vivanta, Guwahati, Assam, India
Time: 10:00AM-10:15AM: Registration Kit distribution/name entry:
10:15AM-11:00AM: Inaugural Session
11:00am-11:30: TEA BREAK
11:30am-12:00pm: Invited Talk by:Prof. Roy Paily Palathinkal, Professor and HOD, Indian Institute of Technology, Guwahati, Assam,India.
12:00PM-12:30PM: Invited Talk by: Dr. Shweta Gupta, ECE, Jain University, Bengalore, India.
12:30PM- 1:00pm: Invited Talk by: Dr. Koushik Guha, NIT, Silchar, Assam.
Technical Session-1:(Time: 1:00pm-2:00pm) (Offline Presentation) (Indian Standard Time)
Session Chair: Prof. Roy Paily Palathinkal, Professor and HOD, Indian Institute of Technology, Guwahati, Assam,India.
Paper Presentation-IDs: 43, 56, 87, 44

2:00PM TO 2:30PM LUNCH BREAK

Technical Session-2 (Time 2:30pm to 5:30pm) (Offline Presentation) (Indian Standard Time)
Session Chair:Dr. Kandarpa Kumar Sarma, Professor,HOD,ECE, Gauhati University, Assam.
2:30PM-3:00PM: Invited Talk by: Dr.Jacoppo Iannacci, Center for Sensor and Devices, Fondazione Bruno Kessler, Trento, Italy.
3:00pm-5:30pm: Paper Presentation IDs: 42, 18, 76, 67, 49, 83, 55, 85, 64, 73
TEA BREAK

========== END OF 1st DAY Program ==========

2nd July 2023: ONLINE PRESENTATION
Technical Session-3: (Time: 2:00pm to 4:00pm) (Indian Standard Time)
Session Chair: Dr. Abhijit Biswas, Professor, Radio Physics and Electronics, University of Calcutta, Kolkata, West Benga.
2:00pm-3:30pm: Paper Presentation IDs: 3, 4, 7, 8, 13, 36(Italy),21, 69(Russia),32, 97.
3:30PM-4:00PM: Invited Talk by: Prof. (Dr.) Sergei Selishchev, Director,
Institute of Biomedical System, National Research Institute of Biomedical Systems
National Research University of Electronic Technology, Moscow, Russia.
Talk Title: Digital twin of implantable total artificial kidney with reabsorption and ultrafiltration imitations: a puzzle

---

2nd July 2023: ONLINE PRESENTATION (Time: 4:00pm to 6:00pm) (Indian Standard Time)
Technical Session-4: (Time: 4:00pm to 6:00pm)
Session Chair:
4:00pm-5:30pm: Paper Presentation IDs: 14, 18, 29, 31, 33, 35, 39, 42, 49, 28(Nigeria),
5:30PM-6:00PM: Invited Talk by: Prof. (Dr.) Abhijit Biswas, University of Calcutta, WB.

2nd July 2023: ONLINE PRESENTATION (6:00PM TO 8:00PM) (Indian Standard Time)
Technical Session-5:(6:00PM TO 8:00PM)
Keynote Talk by:(6:00pm-6:30pm) Dr. Massimo Donelli, Center for Security and Crime Sciences, University of Trento and Verona, Italy.
Session Chair: Dr. Jibitesh Mishra, Professor, Odisha University of Technology and Research, Bhubaneswar, Odisha.
Paper Presentation IDs: 23, 26, 37, 40, 60, 62, 81, 25, 63, 71, 79.

==========END OF 2ND DAY PROGRAM==========

3rd July 2023: ONLINE PRESENTATION
Technical Session-6: (Time: 2:00pm to 4:00pm) (Indian Standard Time)
Session Chair: Dr.Usha Jain, School of Computer Science and Engineering Manipal University, Jaipur, Dehmi Kalan, Jaipur, Rajasthan, India
2:00pm to 2:30pm: Invited Talk by: Dr. Srinivas Rao, ECE, K L University, Guntur, AP.
2:30pm-4:00pm: Paper Presentation IDs: 16, 6. 50, 99, 92

3rd July 2023: ONLINE PRESENTATION
Technical Session-7: (Time: 4:00pm to 6:00pm) (Indian Standard Time)
Invited Speaker:(4:00 to 4:30pm): Dr.Moumita Mukherjee, Professor, Dean(R & D), Adamas University, Barasat, Kolkata, West Bengal.
Session Chair: Dr. Sandip Chandata, GICIET, Maldah, West Bengal. and
Co-Session Chair: Prof. R S Gupta, Maharaja Agrasen Institute Of Technology (MAIT), Delhi.
Paper Presentation IDs: 53, 64, 75, 78, 15, 41, 96, 47,54, 67, 68, 54(Italy), 13, 70, 98(Serberia), 95

3rd July 2023: ONLINE PRESENTATION
Technical Session-8: (Time: 6:00pm to 8:00pm) (Indian Standard Time)
Invited Talk by:
Session Chair: Dr. Moumita Mukherjee, Dean (Research), Adamas University, Barasat, Kolkata, West Bengal. and
Co-Session Chair: Dr. Aminul Islam, Associate Professor, ECE, BIT, Mesra, Jharkhand.
Paper Presentation IDs: 61, 80, 10, 45, 65, 91, 72, 73, 74, 84, 86, 89,94

END OF PAPER PRESENTATIONS
VALEDICTORY SESSIONS (Best paper declarations, publication notice etc.)

Index

Keynote Speaker

Prof. Sergei Selishchev

Director, Institute of Biomedical Systems, National Research University of Electronic Technology, Moscow, Russia.

Talk Title: Digital twin of implantable total artificial kidney with reabsorption and ultrafiltration imitations: a puzzle

Abstracts:

Development of implantable artificial kidneys is an important, perspective aim of modern smart health care and medicine as a means of combating chronic kidney disease. This can be achieved through the creation of radically new, breakthrough technologies based on results of the activities of international consortia and high-risk/high-gain science-towards-technology breakthrough research.

One of these consortia has already been established by the European Commission and started working on the project "Breakthrough technologies for an implantable artificial kidney" on May 1, 2023. It is dedicated to biohybrid technologies that require expensive cell culture techniques for maintenance of the renal cell health. This report is devoted to the planned activities of the Indian-Russian consortium for the creation of implantable total artificial kidneys, without cells. The idea of such consortium was approved by Mr. Subrata Das, the Minister of the Embassy of India in Moscow, during his visit to National Research University of Electronic Technology, Moscow, in October 27, 2022. According to modern ideas, the starting point of designing complex objects is the building of their digital twin. This report will use the methodology of model-based system engineering with the allocation of four stages: the construction of geometric models, the construction of models of physical processes, the construction of behavioural models, the construction of models based on rules. The relationship of these four stages will determine the puzzle of the digital twin of implantable total artificial kidney with reabsorption and ultrafiltration imitations. The natural kidney is a complex object, both in terms of the number and variety of its components, and realizing many physiological functions. Although both the natural and ordinary artificial kidney are excretory organs, each operates on different principle. The natural kidney is a selective filtration with highly selective reabsorption. In contrast, the ordinary dialyzer separates molecular species without reabsorption. Urea, for example, is highly reabsorbed after filtration by the glomerulus, but selective reabsorption plays no role in ordinary dialyzer. Therefore, the initial goal of the Indian-Russian consortium is a digital twin of implantable total artificial kidney with reabsorption imitations. The Indian group has good experience in construction and modelling components for implantable total artificial kidney with reabsorption and ultrafiltration imitations.

The Russian group has a good experience in creating fully finished wearable and implantable medical devices: the first Russian left ventricular assist device, the first Russian wearable artificial kidney. Now the Russian group sets itself the following goal - to design and create an implantable total artificial kidney with reabsorption and ultrafiltration imitations. The integration of the scientific works of the two groups will the world's first digital twin of implantable total artificial kidney with reabsorption and ultrafiltation imitations.

This will open the door to the creation of an appropriate physical prototype. Based on it, the creation of mass production of implantable totally artificial kidneys as microelectronic devices in India and Russia, which will save many lives of patients with chronic renal failure.

Keynote Speaker

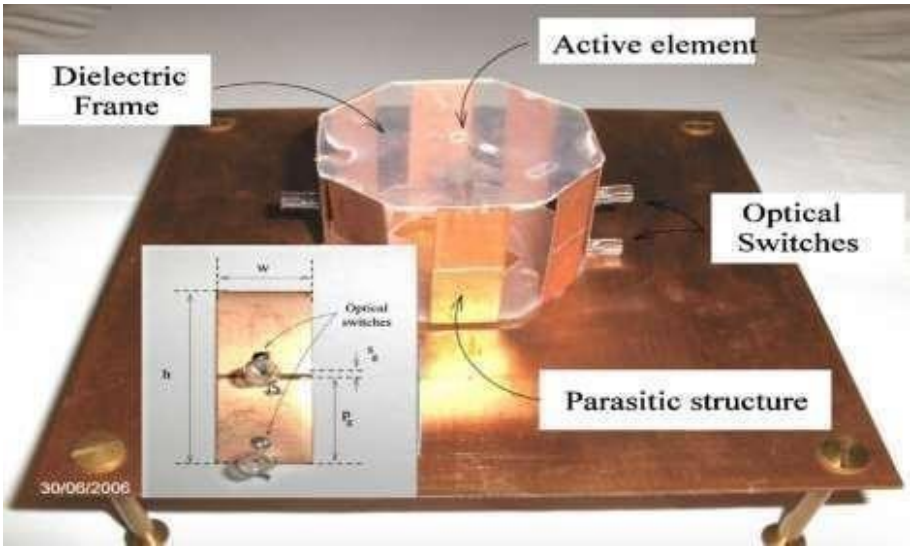
Dr. Massimo Donelli

Center for Security and Crime Sciences, University of Trento and Verona, Italy.

Title: "Unconventional reconfigurable antennas"

Abstract:

Modern mobile telecommunications systems such as mobile smart phones, offer multimedia applications and different services that require a high degree of reconfigurability in spite of the limited dimensions of the devices. In such a framework the design of suitable radiating systems could play a key role in the design of new generations communication systems. The antenna system for 4G devices must be light, cheap and able to keep the devices performances to a high level. In the last decades the use of reconfigurable antennas arrays with fully adaptive properties clearly demonstrated their effectiveness to dramatically improve the performances of a telecommunication system in particular if they are combined with a reconfigurable digital back-end processing unit. Such kind of antennas, commonly used in several fields such as airport surveillance, missile detection and tracking, are unfortunately too much complex, expensive and bulky to be used for commercial portable devices such as mobile phone, and tablets. In this talk different aspects of the use of nonconventional reconfigurable antenna systems, such as parasitic based reconfigurable structures, will be discussed and commented.



Invited Speaker

Dr. Shweta Gupta

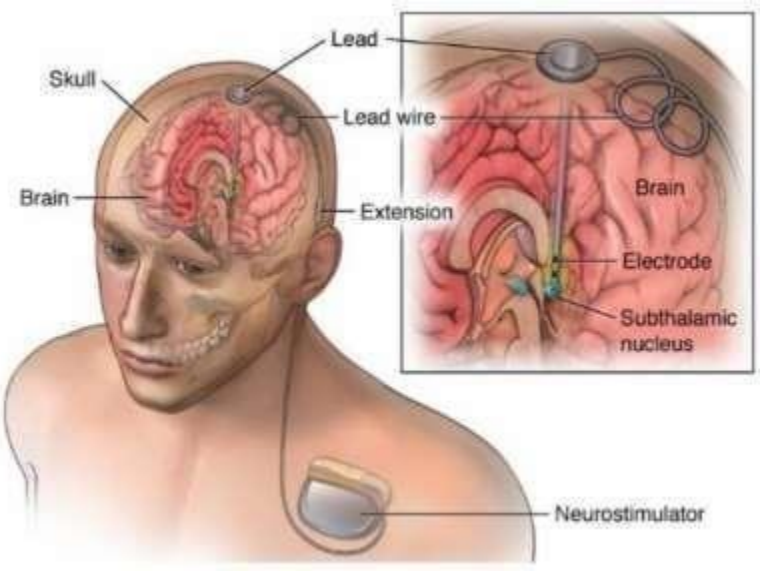
Department of ECE, Jain University, Bengaluru, Karnataka, India.

Abstract:

Deep-Brain-Stimulation (DBS) is a rapidly growing area that aims to enhance the lives of patients with different types of brain disorders. In regards to implanted devices, it's perhaps one of the most active research topics. Power optimization of Low Noise Amplifier (LNA) and DAC used in Closed Loop Deep Brain Neuro-Stimulator (CDBS) at 45nm using Cadence Virtuoso. This study describes a Low-Noise Amplifier (LNA) and Digital-to-Analog Converter (DAC) for biopotential collection on Deep Brain Stimulation. Biomedical signals have a low frequency and milli-volt level noise. Sensors are used to transform these signals into electrical signals. The sensor device is needed to detect biomedical signals produced by the body of humans, such as electromyography (EMG), electroencephalography (EEG), and electrocardiography (ECG). Electric signals from the human body must be transformed into digital signals after they have been detected. Signal processing takes place in the digital realm. In all biomedical applications, an analog-to-digital converter (ADC) is necessary for this conversion. The ADC's primary function is to convert analog signals to their digital equivalents. This digital signal is further processed before being sent out. Low power and extended battery life ADCs are required for these properties. The challenge is to create a low-power ADC with low consumption of power architecture. They should be designed in a way that consumes low power, have a medium resolution, and also has an adequate sampling rate.

Scientists have suggested for years that electroencephalographic (EEG) activity may serve as a communication route between the brain and the computer. Since then, the desire for additional functionality and compactness from technology's electronics has increased. Given the importance of leading with tiny biological signals, an amplifier must be designed which allows these signal components compatible with equipment like as Analog-to-Digital converters for subsequent computer processing. Selective amplification of the raw signal, rejection of superimposed noisy disturbances and interfering signal waves, and protection from harm obtained by higher frequency currents and voltages are all required for the amplifiers.

The neuro-stimulator is a gadget that is about the size of a matchbox, with a battery connected to give power. DBS idea, in which a bio-amplifier (often called a Low-Noise-Amplifier (LNA) and its associated control along with the processing of the signal and its interface electronics receive neural impulses and give stimulation at the same time. The neurostimulator is typically implanted in the chest or abdomen, with the complete device placed beneath the skin with no exposed or visible elements. The symptoms of a variety of illnesses are reduced when the system is turned on, the brain stimulation changes the activity of the neurons in and around the area. Parkinson's disease, 5493 Tremors, Morbid Obesity, Dystonia disorder, obsessive-compulsive disorder (OCD), Tourette Syndrome, and Chronic Pain are among the ailments associated with neurobehavioral and mobility disorders for which other treatments have failed.



Deep Brain Simulation Concept

Because of these factors, as well as the absence of miniaturized devices with the possibilities for safe implant placement on the market, the development of CMOS nanotechnology containing complete DBS systems has enormous social economic implications, in both terms of enabling new treatment techniques and in terms of boosting the market for medical instrumentation and healthcare. This work describes the construction of a CMOS-based Low-Noise Amplifier (LNA) that can record bio-logical signals at a frequency range which is from sub-Hertz to 10 kilo Hertz. The internal architecture of a Closed Loop Deep Neuro Stimulator is used for the treatment of neurological ailments which include obsessive-compulsive disorder (OCD), Epilepsy, Parkinson's disease, Tumors, Chronic Pain, and many more.

Invited Speaker

Dr. Srinivas Rao

General Chair of Micro2023, and Professor, Department of ECE, K L University, Guntur, Andhra Pradesh.

Title: "Dielectrically Modulated Tunnel FET for breast cancer cells: As a Biosensor"

Abstract:

The paper describes a novel biosensor design using a Dielectrically Modulated Full Gate Tunnel Field Effect Transistor (FET) embedded with dual nanocavities. The purpose of this biosensor is to detect cancer cell biomolecules without the need for labelling. The authors conducted simulations using the Silvaco Atlas model to analyze the electrical characteristics of the device in the presence of various cancer cell biomolecules.

The performance of the biosensor was evaluated using several sensing metrics, including current, threshold voltage, and subthreshold slope. These metrics were studied to assess their sensitivity to the presence of different cancer cell biomolecules. By analyzing these metrics, the researchers aimed to determine the biosensor's ability to detect and differentiate between various biomolecules associated with cancer cells.

One crucial aspect discussed in the paper is the incorporation of nanocavities within the biosensor device. These nanocavities are designed to enhance the sensing capabilities of the biosensor. The paper also introduces the concept of the filling factor parameter, which describes the fraction of the nanocavity volume occupied by the cancer cell biomolecules. The filling factor plays a significant role in optimizing the biosensor's sensitivity and performance.

Overall, the paper provides a comprehensive analysis of the proposed biosensor design. The simulations conducted using the Silvaco Atlas model offer valuable insights into the electrical characteristics of the device and its response to different cancer cell biomolecules. The study emphasizes the importance of nanocavities and the filling factor parameter in achieving enhanced sensing performance for cancer cell biomolecule detection.

Keywords: Cancer Cells, biosensor, DMDG Tunnel FET, Nanocavities, TCAD Model.

Keynote Speaker

Prof. Sergei Selishchev

Director, Institute of Biomedical Systems, National Research University of Electronic Technology, Moscow, Russia.

Biography:

Sergey V. Selishchev (Senior Member, IEEE) received the Dipl.-Ing. degree from the National Research University of Electronic Engineering, Moscow, Russia, in 1976, the Ph.D. degree in physics and mathematics from the Institute of Metallurgy and Material Sciences of Russian Academy of Sciences, in 1983, and the Dr. -Sc. degree in physics and mathematics from the Institute of Thermophysics, Russian Academy of Sciences, in 1988.,In 1993, he has initiated the teaching of biotechnical and medical devices and systems with the National Research University of Electronic Technology. In 1999, he has been founded the Department of Biomedical Systems, Institute of Biomedical Systems, since 2018, at this institution and chaired it since foundation. He was the Project Leader in the development of the first Russian automated defibrillator and the first Russian ventricular assist device, namely, Sputnik VAD. He is currently the Director of the Institute of Biomedical Systems, National Research University of Electronic Technology, Zelenograd, Moscow. He has authored and coauthored more than 200 scientific and technical papers. He is also the Editor-in-Chief of the Russian journal Meditsynskaya Tekhnika, translated and published in English as the Biomedical Engineering. *(Based on document published on 7 December 2021).*

Invited Speaker

Prof. Abhijit Biswas

Professor & HOD, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2023).

Biography:

Abhijit Biswas (M'12) received the M.Tech. and Ph.D. degrees from the Department of Radio Physics and Electronics (RPE), University of Calcutta, Kolkata, India. He is currently a Professor with the Department of RPE, University of Calcutta. *(Based on document published on 12 April 2016).*

Keynote Speaker

Dr. Massimo Donelli

Center for Security and Crime Sciences,
University of Trento and Verona, Italy.

Biography:

Massimo Donelli (M'03–SM'12) received the Electronic Engineering and Ph.D. degrees in space science and engineering from the University of Genoa, Genoa, Italy, in 1998 and 2003, respectively. He is currently an Associate Professor of electromagnetic fields with the Department of Information and Communication Technology, University of Trento, Trento, Italy. His research interests include microwave devices and system design, electromagnetic inverse scattering, adaptive antenna synthesis, optimization techniques for microwave imaging, wave propagation in superconducting materials, and urban environment.*(Based on document published on 11 August 2017).*

Dr. Moumita Mukherjee

Dean (R & D), Adamas University, Barasat, Kolkata,
West Bengal, India.
(Ex. Sr. Scientist of DRDO Centre of Excellence) (under Ministry of Defence, Govt. of India).

Biography:

Dr. Moumita Mukherjee is alumni of R K S M Sister Nivedita Girls' School - Kolkata, Presidency College and Calcutta University. She received M.Sc. (Physics) with specialization in Electronics & Communication, M.Tech. in Biomedical-Engineering and Ph.D. (Tech.) in Radio-Physics and Electronics (2009), University of Calcutta, India. She did her doctoral & post-doctoral studies under DRDO, Ministry of Defence, Govt. of India. She received 'visiting scientist' & 'postdoc' positions from INEX, Newcastle University, UK & Technical University, Darmstadt, Germany. Dr. Mukherjee was attached with DRDO Centre under Ministry of Defence, Govt. of India (2009-2015) as Scientist (Reader grade). In continuation to that she joined Adamas University and presently working as Professor – Dept. of Physics & Dean (R&D) after completing her terms as Associate Dean & Academic coordinator (2016-2020), Associate Professor (2017-2020) & Assistant Professor III (2015-2017), in the same University. With a total seventeen years of R&D and teaching experience, she is Visiting / Adjunct Professor of JAP-BMI under Calcutta University and the West Bengal University of Health Sciences. She is empanelled examiner, moderator and PhD supervisor under public & private Universities in West Bengal. She has guided more than 35 Post-Graduate thesis & 12 Ph.D. theses as Supervisor/Jt. Supervisor. Her research interest is focused on THz-electronics, Semiconductor devices, Graphene electronics, Photo-sensors, nano-biosensors and Medical Electronics & instruments. She has published more than 150 peer-reviewed research papers, till date, in reputed international refereed journals and reviewed proceedings with citation globally (citation: 900+, h-index: 16). She is principal investigator of 7 (Seven) Government of India (DRDO) & start-up /industry funded research projects of ~111.30 Lakhs worth.

Keynote Speaker

Dr. Jacopo Iannacci,

Centre for Materials and Microsystems (CMM), Fondazione Bruno Kessler (FBK), Trento, Italy.

Biography:

Jacopo Iannacci (Senior Member, IEEE) was born in Bologna, Italy, in 1977. He received the M.Sc. (Laurea) degree in electronics engineering from the University of Bologna, Bologna, in 2003, and the Ph.D. degree in information and telecommunications technology from the Advanced Research Center on Electronic Systems "Ercole De Castro" (ARCES), University of Bologna, in 2007.,He received the Habilitation as an Associate Professor in electronics from the Italian Ministry of Education, University and Research (MIUR), Rome, in 2017 and the Habilitation as a Full Professor in electronics from the Italian Ministry of University and Research (MUR) in 2021. From 2005 to 2006, he worked as a Visiting Researcher at the DIMES Technology Center (currently Else Kooi Laboratory), Technical University of Delft, Delft, The Netherlands, focusing on the development of innovative packaging and integration technology solutions for radio frequency passives in micro-electromechanical system (MEMS) technology (RF-MEMS). In 2016, he visited as a Seconded Researcher at the Fraunhofer Institute for Reliability and Micro Integration IZM, Berlin, Germany, to conduct high-frequency characterization of RF-MEMS components jointly with the RF and Smart Sensor Systems Department. Since 2007, he has been a Researcher (permanent staff) at the Center for Sensors and Devices, Fondazione Bruno Kessler, Trento, Italy. He has authored more than 130 scientific contributions, including international journal articles, conference proceedings, books, book chapters, and one patent. His research interests and experience fall in the areas of finite-element method (FEM) Multiphysics modelling, compact (analytical) modelling, design, optimization, integration, packaging, experimental characterization, and testing for reliability of MEMS and RF-MEMS devices and networks for sensors and actuators, energy harvesting (EH-MEMS) and telecommunication systems, with applications in the fields of 5G, the Internet of Things (IoT), future 6G, tactile Internet (TI), and super-IoT. Dr. Iannacci has been a member of the Editorial Board of Microsystem Technologies (Springer) since 2015. He is currently an Associate Editor of Microsystem Technologies (Springer) and Frontiers in Mechanical Engineering. He is involved in several international conferences as the Symposium Chair/Co-Chair, the Session Chair, a Technical Program Committee Member, an International Advisory Board Member, a Tutorial Lecturer, and an Invited Speaker, among which the following few are mentioned: IEEE Sensors Journal; IEEE 5G World Forum (5GWF)/Future Networks World Forum (FNWF); Society of Photo-Optical Instrumentation Engineers (SPIE) Micro Technologies; European Solid-State Circuits Conference / European Solid-State Device Research Conference (ESSCIRC-ESSDERC); European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF); International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS).*(Based on document published on 19 December 2022).*

Invited Speaker

Dr. Shweta Gupta

Department of ECE, Jain University, Bengaluru, Karnataka, India.

Biography:

Dr. Shweta Gupta received her B.E Degree in Electronics Engineering in the year 2002 from Pune University and MTech. Degree in Embedded Systems in the year 2005 from BITS Pilani, Pilani, Rajasthan and Ph.D. from Dr. K.N. Modi University, Newai, Rajasthan. She has 14+ years of teaching experience and 6 years of industry experience. She is associated with JAIN (Deemed-to-be University) as an Associate Professor since August 2017. Her research interests include providing medical solutions for Cognitive Diseases especially Epilepsy and Parkinson's Disease using Bionics. To her credit she has published papers in peer reviewed journals and has published three patents with two of them accepted and heading towards their commercialization also. She is an author of a text book titled "Bio-Inspired Algorithms and Devices for Cognitive Diseases using Future Technologies". She is Senior Member of CBEES series of HONG KONG Group of Conferences and has been awarded 100 USD as Session Chair, Invited Speaker, Technical Committee Member and Paper presented in conference ICBBT held in Xian, China in May 16-18, 2022 ,2021 and 2020. She is awarded by AICTE and is with two schemes of AICTE.

Invited Speaker

Dr. Koushik Guha

Associate Dean (Academics), National Institute of Technology, Silchar, Assam, India.

Biography:

Koushik Guha received his B.Tech. Degree in Electronics & Communication Engineering in 2005 from Techno India, Salt Lake, Kolkata under West Bengal University of Technology, India and his M.Tech. Degree in Electronics & Communication Engineering (RF & Microwaves) in 2007 from Burdwan University, West Bengal, India followed by PhD from NIT Silchar in 2016 on "Design and Modelling of RF MEMS Shunt Switch" Currently he is Associate Professor in Electronics & Communication Engineering Dept. at National Institute of Technology, Silchar. Dr. Guha worked as Lecturer in the Dept. of ECE in Haldia Institute of Technology (HIT), West Bengal, India during August 2007 to June, 2010 and served as visiting faculty of NIT Mizoram from 2012 to 2014.He is now an Associate Dean of Students Welfare & Nodal Officer of Scholarships in NIT Silchar. He is awarded Distinguished Faculty Award 2021 by NIT Silchar for his outstanding performance in teaching and research. Recently he has been awarded Institute of Smart Structures and Systems Young Scientist (ISSS, IISc Bangalore) 2021. He is a Fellow of IETE, Senior Member of IEEE, Corporate Member IEI, Fellow InSC, Life member ISSS (IISc Bangalore). He has received number of other awards like "Sardar Vallabhbhai Patel National Reformer Award 2018", "Outstanding faculty in engineering under VIFA 2018", "Institute of Scholar Research Excellence Award 2020", "Institute of Scholar Young Achievers Award 2020" to name a few.

His current research interests include mimicking human body functions using MEMS technology, RF MEMS, BIO-MEMS, Lab on Chip, Organ on Chip, MEMS energy harvesting, design and development of smart sensors for IoT, VLSI circuit design and optimization and many more.

Invited Speaker

Dr. Srinivas Rao

General Chair of Micro2023, and Professor, Department of ECE, K L University, Guntur, Andhra Pradesh.

Biography:

Dr.K Srinivasa Rao was born in Andhra Pradesh, India. He received Master's from BITS Pilani & Ph.D degree from Central University.

-He is presently working as a Professor & Head of Microelectronics Research Group, Department of Electronics & Communication Engineering in Koneru Lakshmaiah Education Foundation (Deemed to be University), Guntur,Andhra Pradesh, India

-His current research areas are

- MEMS based Reconfigurable Antenna's,
- MEMS Actuators,
- Bio-MEMS, Piezoresistive MEMS Pressure Sensor for Gluclose Monitoring etc
- RF MEMS Switches, from L band to 5G Applications
- RF MEMS Filters, RF MEMS Resonators, MEMS Electrospray Thusters for Micro/Nano Satellites
- MOSFET, FINFET(Dual Gtae, MultiGate, Tunnel Gate), VLSI Circuts etc.

-He received Young Scientist Award from Department of Science & Technology, Government of India in 2011.
-He also received UGC Major Research Project from Government of India in 2012.
-He received Early career research Award from SERB, Government of India in 2016.
-Presently he is working on MEMS project worth of 40 Lakhs funded by SERB, Government of India.
-He has published more than 165+ international research publications (IEEE, IET, Springer, Wiley, Elsevier, IOP etc Publishers) and presented more than 65 conference technical papers around the world.
-He is the member of IETE, ISTE, and IEEE. He is Best Teacher Awardee three times in KLU and Best Researcher Awardee in KLU.
-He has organized one International Conference and 12 National Workshops and 5 International/National FDP, each one is partially funded by SERB, ISRO etc.
-SIX (6) Ph.D Research Scholars has been awarded under his guidelines and 8 Ph.D Scholars are working with him.
-He is Reviewer for many SCI indexed Journals(IEEE Transactions, Elsvier, IET, Springer etc.) and also external Reviewer for many universities for M.Tech and Ph.D Program's.

Session Chair and Vidyanagar Awardee

Dr. Kandarpa Kumar Sarma

Professor and Head, Department of Electronics and Communication Engineering, GUIST, Gauhati University, India

Biography:

Dr. Kandarpa Kumar Sarma, currently Professor and Head, Department of Electronics and Communication Engineering, GUIST, Gauhati University, India specializes in computer vision, human computer interaction, cognitive and software defined radio, mobile communication, artificial intelligence, deep learning, speech processing and antenna design. He completed MTech in Signal Processing in 2005 from IIT Guwahati, India. He is a Senior Member of IEEE (USA) and a fellow of Institution of Electronics and Telecommunication Engineers (IETE) (India). Currently he is associated with research in the areas of pandemic compliant smart infrastructure development, AI aided approaches in MIMO-NOMA networks, cognitive electronic warfare and high data rate micro-strip patch antenna designs. Earlier he was associated with the design of high data rate wireless system design using software defined radio. He has been the editor in chief two international journals (International Journal of Intelligent System Design and Computing, Inder science and International Journal of Circuits and Electronics) and Associate Editor of Network: Computation in Neural Systems, Taylor and Francis.

Session Chair and Vidyanagar Awardee

Dr. Prabir Saha

Dept of ECE, National Institute of Technology, Meghalay, India.

Biography:

P. Saha received the B. Tech degree from AMIETE, India, in 2003, and the M.Tech. degree with a major in electronics design and technology from the University of Tezpur, India, in 2008 and the Ph.D. degree in VLSI Design from Indian Institute of Engineering Science and Technology, India, in 2014. He worked as an Assistant Professor in electronics and Communication Engineering Department, in JIS College of Engineering before attending the National Institute of Technology Meghalaya. Since 2012 he has been Assistant Professor in the Electronics and Communication Engineering Department at the National Institute of Technology Meghalaya. His research interests include signal processing, computer arithmetic, VLSI Design, sensor array processing, VLSI array processing, system identification, and digital image processing.

Paper ID: 03

GDI Technique based Full Adder for Enhanced Performance in Computing Applications

Harsh Kumar Bansal, Varun Singh Parmar, Chinta Sharma, Roonak Yaqoob and *Tripti Sharma
Department of Electronics and Communication Engineering,
Chandigarh University, Punjab, India

Abstract:
Nowadays, Ultra-low-voltage (ULV) operation has become more crucial recently in order to reduce energy usage. The fundamental building element of computational arithmetic in many computer and signal/image processing applications is the full adder. Here, a 1-bit new hybrid complete adder circuit that uses both MTV and GDI logic is disclosed. In this materialistic world working with the compact digital appliances/ gadgets, the prime requirement arises for the betterment of the battery life. In order to achieve the prolonged battery life the system should perform with less power consumption. For assuring the high performance of the compact and portable devices processor designs are continuously upgraded with the upcoming new technology. Furthermore, the processing unit and ALUs employ adder circuits to calculate increment or decrement operations, table indexes, addresses, etc., but many other processors also use adder circuits for these purposes.
Keywords- GDI (Gate Diffusion Technique), CMOS (Complementary Metal Oxide Semiconductor), Sub-threshold voltage region and ULV (Ultra low voltage)

Paper ID: 04

A New Circuit-Level Leakage Power Reduction Technique of Static Logic Gates for Analog to Digital Converter in CMOS Technology using Virtuoso

Sufia Banu[1], Shweta Gupta[2]
[1]Research Scholar (Jain University), Assistant Professor (HKBK CE), Bangalore, India,
[2]Associate Professor, Department of ECE, Jain University, Bangalore, India,

Abstract:

The total power in a device is composed of three basic components, having dynamic power due to switching activity, static power while the device in sleep mode and short circuit power while a short amount of current flows from power supply rail (VDD) to ground terminal (GND). The dynamic power component in a CMOS circuit is dominating at lower technology nodes. With scaling, having lesser than 65nm regime the leakage power increases than dynamic power that becomes challenging for the VLSI design engineers. This paper describes a new circuit level leakage power reduction technique called as Input Leakage Controlled Stack Transistor-ILCST for CMOS circuits at circuit level that is been used in 4-bit flash Analog to Digital Converter applicable for deep brain neurostimulator. Analog to Digital Converters (ADC) are crucial for transforming analogue signals from the real world into digital data in the form of 0 and 1. Flash is the most popular ADC owing to its fast speed nature. In this study, a 4-bit flash ADC with a, sample and hold (S/H), comparators and a priority encoder are designed and simulated. To perform sampling process, the sample and hold circuit is utilized. An encoder is a necessary component of a Flash ADC. It converts the comparator output-generated thermometer code (TC) into binary code (BC). The speed, area, and power must all be taken into account while designing the flash analogue to digital converter. Work is implemented using 45nm technology node and carried the simulations in Cadence Virtuoso tool. The static power is reduced significantly using the proposed technique.

Keywords: Deep submicron, Flash Analog to digital converter, Leakage power dissipation, Low power, Static and Dynamic power, VLSI circuit.

Paper ID: 06

Literature review on Non-Invasive Identification of Gastric Abnormalities Using Electrogastrogram

Mirrahashini K [1], Gurumoorthy G[2], Vaideesh Ragavan S[3], Vajeha Jameela S[4], N. Dugra[5]

[1,3,4] Student, Dept. of Medical Electronics, Saveetha Engineering College,
[2]Assistant Professor, Dept. of Medical Electronics, Saveetha Engineering College,
[5] Student, Dept. of Computer Science and Engineering, Sengunthar Engineering College,
[5]Namakkal, [1,2,3,4]Chennai, [1, 2, 3, 4,5,] Tamil Nadu, India,

Abstract:

Electrogastrogram (EGG) records the electrical activity of the stomach muscles, known as slow-wave activity, responsible for rhythmic contractions that move food through the digestive system. The EGG procedure involves placing several electrodes on the skin of the abdomen to detect electrical signals generated by the stomach muscles. EGG parameters commonly analyzed include dominant frequency (DF), percentage of normal activity (PNA), and power ratio (PR), which provide information about the strength and regularity of slow-wave activity. DF refers to the frequency at which the slowwave activity occurs and is typically in the range of 2-4 cycles per minute. PNA is a measure of the proportion of time that slow-wave activity is within the normal range, and PR compares the power of slow-wave activity at different frequencies to detect abnormal patterns of activity. EGG can identify gastric dysrhythmias and diagnose conditions such as gastroparesis, a disorder in which the stomach is slow to empty its contents. EGG can also monitor the effectiveness of treatment for gastric disorders and track changes in slow-wave activity over time. Although EGG has limitations in providing detailed anatomical information or detecting certain types of digestive disorders, it is a valuable non-invasive tool for evaluating gastric function.

Keywords— Electrogastrogram (EGG), electrical activity, stomach muscles, slow-wave activity, rhythmic contractions, digestive system, electrodes

Paper ID: 07

Design and Development of Ultra-lightweight Block Cipher Architecture for IoT Resource Constrained Devices

Mihir Lal Saha, Dr. Krishna Lal Baishnab, Siddartha Roy, Dr. Koushik Guha, Sourav Nath, Dr. Gaurav Singh Baghel
Department of Electronics and Communication Engineering National Institute of Technology, Silchar Assam, India

Abstract:

The rapid growth of IoT devices has led to an increasing need for security solutions that can be implemented in resource constrained environments. In this work, we propose a ultra lightweight block cipher architecture for IoT devices that provides strong encryption while minimizing the required computational resources. A comparison of the proposed circuit's different attributes with those of the existing block ciphers such as gate equivalent area, power consumed by the proposed architecture, and delay are calculated and presented in a tabular form. The simulations and synthesis part has been done using Xilinx ISE 14.7 and Cadence tools. The construction of the proposed architecture requires only 960 Gate Equivalents (GE). Which is lesser than many existing block ciphers. It can be called an Ultra-lightweight block cipher as its Gate Equivalents (GE) is lesser than 1000[22]. Power consumption of proposed architecture is 0.53 mW which is lesser than many existing block ciphers. Delay is also improved as compared to many block ciphers.

Keywords—Block cipher, IoT resource constrained devices, Ultra- light weight, Xilinx, Cadenc.

Paper ID: 08

Wireless Adhoc BLE Mesh for Smart Home Applications

Koushik Guha[1], Lakshmi Narayana Thalluri[2], Pavan Sai Sajjala[2], Srikanth Ganji, Balarama[2] Krishna Sai Damarala[2]
[1]National MEMS Design Center, Department of Electronics and Communication Engineering, National Institute of Technology, Silchar-788010, Assam, India.
[2]Department of ECE, Andhra Loyola Institute of Engineering and Technology, Vijayawada-520008, A.P., India.

Abstract:

A recently created energy-efficient short-range wireless communication technology is called Bluetooth Low Energy (BLE). BLE is increasingly common and well-liked in Internet-of-Things (IoT) applications. The quantity of deployed BLE devices has increased as a result of this. Applications use connectionless communication, in which nodes broadcast information using advertisement messages to ensure energy efficiency. The highest peer-to-peer throughput, the most significant distance that a mesh network can span, and the security features of the BLE Mesh are all discussed and compared in this study. This suggests a connectionless BLE communication protocol that increases communication effectiveness in IoT applications where numerous BLE nodes operate in the same space and communicate with a central server simultaneously. A typical application that uses a passive scanning mode is contrasted with the proposed scheme, which is based on an active scanning mode. A wide range of IoT applications can use the proposed connectionless BLE communication scheme to enhance their performance and coexistence with other 2.4GHz-band devices. The proposed communication plan also has minimal costs and implementation complexity.

Keywords – BLE, Mesh Topology, Advertising.

Paper ID: 10

Design & Implementation of a Meta-Material Based Ultra-Wide Band Microstrip Patch Antenna for Vehicular Communication

Purnima K Sharma[#1], Jerzy R. Szymański[#2], inż. Marta Żurek-Mortka[#3], Mithileysh Sathiyanarayanan[#4]
[#1]Postdoctoral Fellow, Kazimierz Pulaski University of Technology and Humanities in Radom, Poland, Europe
[#1]Sri Vasavi Engineering College, Tadepalligudem-534101, India
[#2]Faculty of Transport, Electrical Engineering and Computer Science, Kazimierz Pulaski University of Technology and Humanities, 26-600, Radom, Poland.
[#3]Department of Control Systems, Lukasiewicz Research Network-Institute for Sustainable Technologies, 26-600, Radom, Poland.
[#4]MIT Square, London

Abstract:

This revolutionary tiny microstrip antenna that is built using meta-materials is described for UWB applications. The antenna comprises of two surfaces of meta-materials that were created by engraving pi-shaped slits and cross-shaped slits on the radiating plane and the ground plane, individually. The left-handed activity of such meta-material is caused by the combination of capacitive and inductive effect created by the radiating plane and ground plane, together. The proposed structure is 30.8 x 27.6 x 0.8 mm^3 in shape and is supplied by a 50Ω feed line that is connected via a SMA connector. The electrical resistance ranges from 3.5GHz to much greater than 14.5GHz, with maximal emission along the reference axis as well as a directed pattern that directly helps with frequency. The aim of designing this antenna is to facilitate seamless communication between vehicles, which demands a wide frequency range for establishing uninterrupted connectivity in vehicular communication applications.

Keywords: Metamaterial antenna, Dual-band, Optimum s11 Parameter, Ultra-Wide Band.

Paper ID: 13

Graded JAM Split Gate-All-Around (GJAM-SGAA) Bio-FET for Label Free Avian Influenza Antibody and DNA Detection

Shivani Yadav, Sonam Rewari
Electronics & Communication Engineering Department
Delhi Technological University Delhi, India

Abstract:

This manuscript presents a novel biosensor design called Graded JAM Split Gate-All-Around (GJAM-SGAA) Bio-FET for the detection of Avian Influenza antibody and DNA biomolecules. The GJAM-SGAA Bio-FET utilizes a silicon Gate-All-Around FET which operates in the Junction less Accumulation Mode (JAM), with a graded doping in the channel divided into three regions. This Bio-FET also features a gate underlap cavity (open cavity) that enables the immobilization of the biomolecules to be detected without the use of labels. The GJAM-SGAA Bio-FET offers a sensitive and reliable approach for disease diagnosis. Three independent cylindrical gates have been used to realize gate metal engineering. Gate underlap cavities overcome the fabrication complexity of nano meter range nanocavities in FET biosensors and provides structural stability. Also, the graded JAM and Gate Metal Engineered FET structure significantly improves the device performance and detection sensitivity. A comparative analysis between the GJAM-SGAA BioFET and a biosensor based on the Junction less Split Gate-All-Around FET (JL-SGAAFET) have been performed to evaluate their respective performances. The proposed BioFET, when compared to a JL-SGAAFET Biosensor, has 5.72 times higher ION current sensitivity, 5.3 times increase in threshold voltage sensitivity, and 2.13×102 times improvement in switching ratio sensitivity for the case of Avian Influenza biomolecule immobilization in the cavity region, while for DNA biomolecules it has 1.64 times higher ION current sensitivity, 5 times increase in threshold voltage sensitivity, and 1.05 ×102 times improvement in switching ratio sensitivity.

Keywords— Graded JAM, Split Gate-All-Around, GJAM-SGAA, Gate Underlap Cavity, detection Sensitivity.

Paper ID: 14

Design of 256 bytes 10T SRAM for low power portable device applications

Priyanka. N[1], Rachana. S[2], Sai Varun Reddy. K[3], Chandramauleswar Roy[4]

Department of Electronics and Communication Engineering Madanapalle Institute of Technology and Science Madanapalle, India[1, 2, 3], IEEE Member School of Electronics Engineering. Vellore Institute of Technology, Chennai, India[4].

Abstract:

This article presents designing of 256 Bytes SRAM cell for low power applications. The important design parameters of proposed 10T (PROP10T) and others conventional SRAM cells are evaluated using HSPICE Monte Carlo simulations at 22nm technology node. The estimated results are contrasted with those obtained using conventional 6T (CONV6T) SRAM cell, conventional 7T (CONV7T) SRAM cell, conventional 8T (CONV8T) SRAM cell, conventional 9T (CONV9T) SRAM cell, and conventional 10T (CONV10T) SRAM cell. The Read Static Noise Margin (RSNM) of proposed 10T is same as CONV6T, CONV8T, CONV9T, CONV10T and more than 37% as compared to CONV7T. The Write Time of PROP10T is 1.2 times lower as compared to CONV 8T and 1.2×/1.19×/1.21×/1.21 higher as compared to CONV6T/CONV7T/CONV9T/CONV10T. The Read Time of PROP10T is 1.2 times lower as compared to CONV7T and 1.13×/1.53×/1.14×/1.26 higher as compared to CONV6T/CONV8T/CONV9T/CONV10T.The Hold Power of PROP10T is 55×/15×/55×/55×/157 lower as compared to CONV6T/CONV7T/ CONV8T/CONV9T/CONV10T. The Write Power of PROP 10T is 6.2×/1.68×/7×/4.2×/2.1 higher as compared to CONV6T/CONV7T/ CONV8T/CONV9T/CONV10T. Write Static Noise Margin (WSNM) is high for proposed 10T (PROP10T) compared to other conventional SRAM cells.

Keywords: Read Access Time, Write Access Time, Write Static Noise Margin (WSNM), Read Static Noise Margin (RSNM), Hold Power, write power

Paper Id: 15

Design of low leakage and Highly Speed 10T SRAM in 22nm Technology node

Ravi Kumar D, Ramakishore Reddy B, Jyothi P, Chandramauleshwar Roy

Department of Electronics and Communication Engineering,
Madanapalle Institute of Technology & Science (MITS) Madanapalle, Andhra Pradesh, India

Abstract:

This article presents a low leakage and highly proposed 10T (PROP10T) SRAM cell. The HSPICE Monte Carlo Simulations are used to measure the critical design metrics of proposed 10T SRAM cell. Estimated results are compared with the conventional 6T (CONV6T) SRAM cell and Transmission Gate based 8T (TG8T) SRAM cell. The write delay (TWA) of PROP10T achieved 4.2×/1.3× less in comparison to CONV6T/TG8T respectively. The PROP10T has shown 1.08× less than CONV6T and 1.4× higher read delay (TRA) as compared to TG8T SRAM cell. The leakage power of PROP10T consumes 6.85× lower then CONV6T but at the cost of TG8T SRAM cell. The layout designed and area calculation done using Micro wind, the proposed 10T SRAM occupies 1.24× larger area as compared to TG8T and occupies 2.23× larger area as compared to the CONV6T due to higher number of transistors.

Keywords: Read Access Time, Write Access Time, Read Static Noise Margin (RSNM), Hold Power.

Paper Id: 16

Hyperspectral image compression using prediction-based band Reordering Technique

S Nithya, Dr. Shweta Gupta

Department of Electronics Engineering, faculty at SJB Institute of technology, Department of Electronics and Communication Engineering, Jain University, Bangalore – 562 112, INDIA

Abstract:

The hyperspectral image represents various spectral characteristics because it contains multiple spectral information of ground materials that can be used for various applications. These images are captured as huge data and need to process and transfer to the ground station. These captured images contain redundancy spectral information that needs to compress to reduce the transmission capacity and storage. This paper focuses to preserve their quality using band reordering Techniques and prediction coding for compression. This can be achieved by preprocessing in this sub-bands decomposition are done and bands are reordered into unsequenced compression can be achieved by using linear prediction. The paper deals with the hyperspectral image datacube of Pavia University which was captured by a sensor known as reflective optics system imaging spectrometer (ROSIS-3) over the city of Pavia, Italy.

Keywords: Hyperspectral image, compression techniques, transformation-based techniques, prediction-based techniques, band reordering, Evaluation parameters.

Paper Id.: 18

Improved Design MEMS Cantilever Biosensor for Tuberculosis Detection

[1] Laipang Brahma, [2] Dr. Koushik Guha (Associate Professor), [3] Prof. (Dr.) K. Srinivasa Rao

[1 ,2, 3] Department of Electronics and Communication
[1,2] National Institute of Technology Silchar, India,
[3] KL University, Guntur Andhra Pradesh, India

Abstract:

In this paper, MEMS cantilever beam bio-sensing system is simulated, analyzed and designed for quick tuberculosis detection using Intellisuite Software. The surface of the cantilever has been coated with antibodies, which bind to the antigen present. The surface is strained and forms deflection once the target molecules are discovered. A variety of models were designed from different materials with varying lengths, widths and shapes of the cantilever to improve displacement and sensitivity. To improve the performance of the cantilever, Stress concentrating region (SCR) designs is included. Materials analyzed in this paper were silicon, gold, polydimethylsiloxane (PDMS) and polyimide. The highest displacement achieved 4.59 × 10−2μm with PDMS material for length 300μm, width 50μm and thickness 0.5μm. Improved displacement achieved 9.30 × 10−2μm with PDMS using SCR Model-2 for length 300μm, width 50μm and thickness 0.5μm. Among shape variants, T-shaped is found to be achieved the highest displacement. For limited size and compact design biosensors modified improved model is designed with a combination of SCR Model-2 and T-shaped with length 200μm which produces the highest displacement of 5.44 × 10−2μm. The readout method for biosensor design is done in MATLAB Simulink. Piezoelectric material Lead Zirconate Titanate (PZT5A) is also used to provide an output voltage. PDMS is discovered the highest displacement and voltage among the other three materials.

Keywords: Tuberculosis (TB), MEMS, Cantilever, Antigen, Antibodies, SCR, PZT-5A

Paper Id.: 21

Mathematical Modeling and Analysis of Nanosphere structure for Bio-Sensing Application

Suryanarayana N K[1], Asha K[2], Narayan Krishnaswamy[3], Koushik Guha[4], Venkatesha M[1]

[1]Department of ECE, Sai Vidya Institute of Technology, Bengaluru, Karnataka – 560064, INDIA
[2]Department of ECE, BMS Institute of Technology & Management, Bengaluru, Karnataka – 560064, INDIA
[3]Department of AI & ML, Nitte Meenakshi Institute of Technology, Bengaluru, Karnataka – 560064, INDIA
[4]Department of ECE, National Institute of Technology, Silchar, Assam – 788010, INDIA

Abstract:

Nanosphere structure are the suitable and efficient nanoparticle for the biological application in designing the refractive index-based sensors. Mathematical modeling and analysis of Nanosphere structure is simulated and modeled. Nanosphere structure acts as a surface plasmon device. The Gold nanospheres are commonly used nano devices. The visible spectrum wavelength from 300 nm-900nm is applied in this example. The Mie scattering algorithm and dipole approximation methods are the modeling methods used. The cross-section efficiency and sensitivity of the nanosphere based refractive index sensor is analyzed.

Keywords: Nanosphere, Surface Plasmon Resonance, Nanoparticle, Absorption, extinction, scattering.

Paper Id.: 22

Design of Power efficient 10 T SRAM Cell

[1] B. Praveen, [1] P. Praveen, [1] Chandramauleshwar Roy, IEEE Member, [2] B. Rama Mohan

School of Electronics Engineering, Vellore Institute of Technology, Chennai-600127, TN, India
Department of Electronics and Communication Engineering Madanapalle Institute of Technology and Science Madanapalle-517325, AP, India

Abstract:

This paper presents a 10T SRAM cell that is based on CMOS technology and reduces leakage power, write power and write delay considerably as compared to conventional 6-transistor (CON6T) SRAM cell and conventional 10-transistor (CON10T) SRAM cell. The simulated result of proposed 10T SRAM cell shows 10.2×/13.95× improvement in write power as compared to CON6T/CON10T SRAM cell respectively. Our proposed 10T SRAM cell shows 31.68×/1.16 improvement in standby power as compared to CON6T/CON10T SRAM cell respectively. The simulated result of our proposed 10T SRAM cell shows 1.08×/1.08× faster read access time as compared to CON6T/CON10T SRAM cell. Ananlysis has been done in the subthreshold voltage range and analysis shows significant improvement in leakage power when compared to the conventional 6T and conventional 10T SRAM cell.

Keywords: Leakage Power, write delay, read delay, write power, read power, ultra low power design.

Paper Id.: 23

Effect of on-Air time on the Performance of Low Range Wide Area Network (LoRaWAN)

Srishti Sabharwal, Prabhjot Singh

Electronics and Communication Departments, Chandigarh University, Mohali, India

Abstract:

In the present Internet of Things industry, LoRa is a proficient technology that uses ultra-powerful devices and unlicensed bands to provide long-range communications. In order to evaluate the functioning of the network, it is critical to ascertain the collision rate. By examining the potential amount of packet collisions, the current article intends to evaluate the performance level of LoRaWAN technology. This paper discusses Lora, its architecture, evaluation, and the effect of the spreading factor (SF) on the on-air time parameter. The paper also presents the trade-off between Air-time and a spreading factor. Analysis shows that the lesser the spreading factor lesser will be the time on air. Hence, the chances of errors in communication are reduced.

Keywords: On-Air time, LoRa, LoRaWAN, Spreading Factor, Data Rate

Paper Id: 25

A mixed technique for order abatement of Linear time invariant System

Priyajit Dash[1], M. L. Meena[2], Afzal Sikander[3]

[1]Research Scholar, Department of Electronics Engineering, Rajasthan Technical University, Rawatbhata Road, Kota-324010 (Rajasthan), India. dash.priyajit@gmail.com
[2]Assistant Professor, Department of Electronics Engineering, Rajasthan Technical University, Rawatbhata Road, Kota-324010 (Rajasthan), India. mlmeena@rtu.ac.in
[3]Assistant Professor, Department of Instrumentation & Control Engg., Dr B R Ambedkar National Institute of Technology, Jalandhar, India. afzals@nitj.ac.in

Abstract:

In this work, a new mixed technique has been proposed for Order Abatement (OA) of the Linear Time-Invariant (LTI) system. The numerator polynomials are calculated by Stability Equation (SE) and the denominator polynomials are Honey Badger Algorithm (HBA). Here Integral Square Error (ISE) has been considered as an objective function for OA to minimize the error between the High Order System (HOS)/ Original System and the proposed Abated System (AS) to find its unknown coefficients The result obtained from tested examples clearly shows the superiority of the proposed technique. Various performance indices and transient parameters have been compared with the proposed method and recent popular techniques from the literature.

Keywords: Stability Equation, Honey Badger Algorithm, Integral Square Error, Meta-Heuristic Optimization Algorithm, Order Abatement, Abated System

Paper Id.: 26

A Review of Hybrid Electric Vehicles Franchising

Saritha Kumari Thumma, Dr Sayanti Chatterjee, Dr P Sridhar, A Satish Kumar, Dr M Laxmidevi R

Department of Electrical & Electronics Engineering Institute of Aeronautical Engineering, Hyderabad , INDIA

Abstract:

This paper presents the foreword of EVs which signals commencement to the ending for conventional vehicles which have engines. The chief inspirations to changing to electric vehicles are the willingness to plummet harmful gases and dropping reliance on fossil fuels. At the closure of this year, the universal stockpile of electric vehicles will be few millions. Rising recognition of electric vehicles will facilitate quite a lot of factors: scientific advancements, growing storage space capability of power storage devices joined by declining price, amplified charge station amenities and benefits from the government. Electric vehicles which are presently lingered in peak are vehicles which employ batteries (BEV), second are electric vehicles which use hybrid technologies. The future of electric vehicles their restrictions and different mechanisms used in electric vehicles are discussed in thisreport.

Keywords: electric vehicles, batteries, motors, franchising, key barrie

Paper Id.: 28

RFID Library Management System Dependability through Reliable Fault-Detection and Fault Correction Procedures

Nicholas Ude Eze[1], Ekene Ozioko[2], Johnpaul Nwigwe[2], Koushik Guha[3]

[1]Department of Computer and Robotics Education, University of Nigeria, Nsukka – 234, NIGERIA
[2]Department of Computer Science Enugu State University of Science and Technology, Enugu – 234, NIGERIA
[3]Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, India

Abstract:

Apart from the widespread acceptance of the digital library as a major research response among university lecturers and students, little is known about the reliability of its RFID management software (RFIDMS), the challenges posed during software flaws, and the improvement strategies that can be used to maintain the RFID software reliability. The various NHPP software reliability growth models (SRGMs) to investigate the reliabilities of software products of this kind in real-world software development has not always been achieved because those studies were primarily concerned with modeling fault detection processes (FDP) and ignoring the fault correction processes (FCP). Here, we propose a reliability model of RFID software while keeping in mind the interdependence between fault quantities of the dual procedures of fault detection and fault correction. In evaluating the software reliability, fault introduction and testing coverage rates were included to the parameters making our proposed model to be highly effective in estimating and forecasting the dependability of the software when compared with existing NHPP software reliability growth models (SRGMs).

Keywords: Digital Library Management Software (DLMS), Fault Detection, Fault Correction, Imperfect Debugging, RFID, Testing Coverage, Software Reliability.

Paper Id.: 29

Compact and Novel Structure Substrate Integrated Waveguide Antenna for millimetre wave 5G Applications

G Naveen Kumar[1] , Anusha Yellapu[2] , Dr. Y V Narayana[3] , Dr. Koushik Guha[4] , Dr. Srinivasa Rao Kanumuri[5] , Dr. Kavicharan Mummaneni[6] .

1. Associate professor, Dept. of ECE,VVIT, Guntur.
2. Research Scholar, Dept. of ECE, NIT Silchar,
3. Professor, ECE Department, Tirumala Engineering College, Narsaraopeta
4. Associate Professor, Dept. of ECE, NIT Silchar.
5. Professor, Dept. of ECE, KLU.
6. Assistant Professor, Dept. of ECE, NIT Silchar.

Abstract:

A new single structure stair-case steps slot Substrate Integrated Waveguide (SIW) antenna is designed and analysed in this work. The overall dimension of the current design compact structure filled an area of 11 mm × 10 mm. The receiver is excited by grounded coplanar waveguide transmission (GCPW). The performance parameters like reflection coefficient, VSWR, radiation patterns etc. at 26 GHz are studied and given in this paper. For the suggested design the reflection coefficient parameter which is ≤ -10 dB over the entire operating band of resonant frequency. The proposed Antenna can be applied for mm wave 5G applications. The bandwidth measured is around 1GHz at the resonant frequency which makes it better applicable for the system of 5G communications and various wireless applications which require high bandwidth.

Keywords: Stair-case steps slot, substrate integrated waveguide, GCPW, mm wave, 5G communications and wireless applications.

Paper Id.: 31

Implementation of Full Adder using mCell

Anurag Chauhan, Shivank Sharma, Shorya Kumar, Shreyas Jain

Department of Electronics and Communication
Delhi Technological University, Delhi– 110042, INDIA

Abstract:

The issue of leakage power has become a substantial issue in the scaling of CMOS technology. Magnetic Cell (mCell) based logic is a hopeful approach as it occupies a lesser area, is non volatile and has negligible static power consumption. This paper gives forward a design for a full adder that is made using mCell logic without the need of intermediate circuitry. Simulation reveals that very less power is used in the design, fewer elements and a very low Power Delay Product (PDP) which is less than 2% of a conventional CMOS based Full Adder's PDP.

Keywords: Spintronic logic devices, Magnetic Tunnel Junction (MTJ), Magnetic Cell (mCell)

Paper Id.: 32

DESIGN OF MPPT USING INTELLIGENT SYSTEM FOR HYBRID WIND SOLAR PV PLANT

Subhasis Bandopadhyay[1], Atanu Bandyopadhyay[2], Ashoke Mondal[3], Pradip Kumar Sadhu[4]

[1, 2] National Institute of Technology, Shillong, Meghalaya, India.
[3] RCC Institute of Information Technology, Kolkata, India.
[4] IIT Dhanbad (ISM)

ABSTRACT:

Renewable energy sources have become a popular alternative electrical energy source where power generation in conventional ways is not practical. In the last few years, the photovoltaic and wind power generation have been increased significantly. In this study, we proposed a hybrid energy system which combines both solar panel and wind turbine generator as an alternative for conventional source of electrical energy like thermal and hydro power generation. A simple intelligent battery charging system which is also cost effective with a effective MPPT algorithm has been proposed to track and monitor the operating point at which maximum power can be coerced from the PV and wind turbine hybrid system under continuously changing environmental conditions. The entire hybrid system is described given along with comprehensive simulation results that discover the feasibility of the system. A hardware simulation model has been developed on a small scale to demonstrate our ideas

Keywords: Wind solar PV plant, Mppt algorithm, fuzzy logic method, simulation mode, hardware model, Result analysis

Paper Id.: 33

Comparative analysis of different DC-DC converters for solar PV system

Kamaldeep Singh, Rahul Bisht, Afzal Sikander, and Narinder Singh Bhangal

Department of Instrumentation and Control Engineering
Dr. B. R. Ambedkar, National Institute of Technology, Jalandhar, India

Abstract:

Solar power has evolved as a competitive alternative to conventional energy sources in response to the growing demand for renewable energy sources. But the amount of sunlight and temperature affect the power generation of solar panels. Therefore, a DC-DC converter is required to transform the solar panel's variable DC output into a constant voltage level. To effectively convert DC voltage levels, DC-DC converters are widely employed in a variety of power electronics applications. However, the performance and efficiency characteristics of various converter topologies vary. In this paper, the model of various DC-DC converters are developed and evaluated for the solar PV system. The efficiency of different DC-DC converter such as buck, boost, buck-boost, cuk and sepic converter is compared in this paper, when used with a solar panel as the input power source. Further, the considered converters have been evaluated and compared under different operating conditions such as variable load resistance, temperature and irradiance are taken into account in the analysis.

Keywords: DC-DC Converter, efficiency, renewable energy, PV system.

Paper Id.: 35

A Novel Low Power Design Circuit Approach with Enhanced Positive Feedback Adiabatic Logic Reginald

H. Vanlalchaka[1], Reshmi Maity[2] , Lalthanpuii Khiangte[3] , Niladri Pratap Maity[4]

[1, 3] Department of Electronics, Govt. Zirtiri Residential Science College, Aizawl, INDIA
[2, 4] Department of Electronics & Communication Engineering, Mizoram University (A Central University), Aizawl, INDIA

Abstract:

This paper offers a unique novel adiabatic logic family for low-power uses named "Enhanced Positive Feedback Adiabatic Logic" (EPFAL). Recommended circuit offers two complementary outputs since it is constructed on dual-rail encoded and sense-amplifier-structured quasiadiabatic circuits. The proposed concept substitutes a four-phase trapezoidal power clock with a two-phase split-level sinusoidal power clock. The simulations were performed using Cadence Virtuoso, utilizing the Low Power Berkeley Predictive Technology Model (45 nm LP_PTM) at various operating frequencies. This study uses a number of reference transistor-based adiabatic logic families, such as Efficient Charge Recovery Logic (ECRL), Positive Feedback Adiabatic Logic (PFAL), 2N2N2P, Two Phase Positive Feedback Adiabatic Logic (2P-PFAL), Improved Pass Gate Adiabatic Logic (IPGL), Differential Cascode Pre-resolve Adiabatic Logic (DCPAL), Clocked Differential Cascode Adiabatic Logic (CDCAL) and, Adiabatic Differential Cascode Voltage Switch Logic (A-DCVSL).

Keywords: VLSI, EPFAL, CMOS, LP_PTM, Adiabatic Logic.

Paper Id.: 36

On Chip Modulated Scattering Tag operating at Millimetric Frequency Band

Irene Dal Chiele[1], Massimo Donelli[2], Jacopo Iannacci[3], Koushik Guka[4]

[1]Department of Civil, Environmental and Mechanical Engineering (DICAM), University of Trento, Trento 38123, Italy. [2]Center for Security and Crime Sciences, University of Trento and Verona, Italy. [3]Center for Sensors and Devices (SD), Fondazione Bruno Kessler (FBK), Trento, Italy. [4]Department of Electronics and Communication Engineering, National Institute of Technology (NIT) Silchar, Assam-788010, India.

Abstract:

A miniaturized modulated scattering technique (MST) tag operating at millimetric frequency bands is proposed in this work. In particular, the proposed tag operates like a RFID tag, but thanks to the MST technique it does not require a radiofrequency front end. The information is carried on by modulating an interrogating electromagnetic wave with a suitable change of impedance of the tag antenna obtained by means of a RF-MEMs switch. With respect to standard RFID tags, with a limited operative range, MST tags can theoretically reach any operative range up to kilometers. All the components of the MST tag are directly designed on-chip leading to a very compact design. The tag has been designed to operate at millimetric frequency bands at about 70GHz. The preliminary experimental results are quite promising and they demonstrated the capabilities and potentialities of this technique.

Keywords: Modulated Scattering Technique (MST) tag, on-chip antennas, RF-MEMS,·RFIDs

Paper Id.: 37

Automatic Self-Balancing Robot for Crop Monitoring

Rachel Shukla, Anand R, J Ramprabhakar

Department of Electrical and Electronics Engineering Amrita School Of Engineering Bangalore,
Amrita Vishwa Vidyapeetham, India
Karnataka, India

Abstract:

The Automatic Self Balancing Robot for Monitoring of Crop is a novel robotic system designed for the agricultural industry to improve crop monitoring and management. The robot is equipped with sensors, cameras, and machine learning algorithms that enable it to navigate through fields, collect data on plant health, and identify potential issues here in this case fruit ripening (Early ripe, partially ripe, Ripe and Decay) with the help of camera. The self-balancing feature of the robot allows it to operate on uneven terrain, ensuring stable and accurate data gathering. Data gathered by the robot such as temperature, humidity and soil moisture are sent to a central system for analysis, enabling agricultural producers to decide on crop management. The use of this robotic system can increase productivity, reduce employment costs, and improve overall harvest yields.

Keywords: Self-balancing robot, SVM, KNN

Paper Id.: 39

Analysis of Total Harmonic Distortion Reduction in Hybrid Boost Converter fed BLDC motor

Sunam Saha[1], Debjyoti Chowdhury[2], Madhurima Chattopadhyay[3], Moumita Mukherjee4 [4]

[1, 4]Adamas University, Kolkata, West Bengal
[2,3] Heritage Institute of Technology, Kolkata, West Bengal

Abstract:

Brushless DC (BLDC) motor has become an attractive choice in various industrial and domestic applications because they offer wide range of speed and torque. Since, BLDC motors relies on electronic commutation, inherent problems of power electronic circuits like harmonics significantly affects the motor performance. Moreover, application of DC-DC converter in BLDC drive introduces non-linear phenomenon. In this article, a mathematical analysis has been performed to analyze the change in the total harmonic distortion in electromagnetic torque of BLDC drive with the change in the inductance of the hybrid boost converter. A power spectrum analysis has been presented on the output voltage of the hybrid converter with change in inductance. It has been observed that with decrease in inductance the total harmonic distortion of electromagnetic torque reduces.

Keywords: DC-DC converter, BLDC motor, THD, power Spectrum

Paper Id .: 40

Simple, Secure and Lightweight Authentication Protocol with Session-Key Generation for IIoT Device in IIoT Networks

Usha Jain[1], Sunil Kumar[2], Gireesh Kumar[3], Aprna Tripathi[4]

[1, 2, 3] Department of Computer Science and Engineering, Manipal University Jaipur, Rajasthan-303007, India
[4] Department of Information Technology, Manipal University Jaipur, Rajasthan-303007, India

Abstract:

The Industrial Internet of Things (IIoT) has led to a growing number of connected devices, making device authentication a critical aspect of securing IIoT networks. In this paper, we offer a unique method for IIoT device authentication that makes use of XOR and hash functions, two lightweight cryptographic methods. To improve the security of IIoT devices in IIoT networks, our method uses authentication and session key generation. In this suggested protocol, IIoT devices ask a server for authentication via a message, and the server replies with session keys. The IIoT device updates the session key and saves it for use in subsequent communications to ensure secure connection. We modelled our proposed protocol on AVISPA (Automated Validation of Internet Security Protocols and Applications) and Proverif tools. Our proposed protocol's results show that this protocol provides a secure and efficient method for IIoT device authentication with minimal communication, computational and storage overheads.

Keywords: Device authentication, Industrial Internet of Things (IIoT), session-key generation, security, secure communication

Paper Id.: 41

The application of Space Vector PWM technique using In STATCOM to reduced harmonics injection by Grey Wolf Algorithm

Subhasis Bandopadhyay[1], Atanu Bandyopadhyay[2], Ashoke Mondal[3], Pradip Kumar Sadhu

[1] National Institute of Technology, Shillong, Meghalaya, India.
[2] RCC Institute of Information Technology, Kolkata, India.
[3]IIT Dhanbad (ISM).

Abstract:

Power quality improvement is one of the major challenges in power transmission and distribution systems. A novel method is proposed in which a multi-level converter is developed with a reduced number of switches. A new model of 12-Pulse 5.2kV, 25MVAr converter controlled by state vector modulation technique is proposed. The output voltage waveform of the converter contains the 11th, 13th, …23rdand 25th order of harmonics. In the present work, a coupling transformer is used to minimize lower harmonics existing in converter output. Further switching angle optimization algorithm is adopted to minimize higher-order harmonics. The optimization of THD percentage obtained by the Grey-Wolf method is compared with Particle Swam optimization. In this paper, a multi-level GTO-converter is found to achieve a THD reduction of up to 4.12%. The switching angle optimization in the D-SPACE environment resulted in THD reduction. The voltage waveform is improved and at the same time injection of reactive power to the utility Grid is decreased.

Keywords: 12 pulse STATCOM, Power quality improvement, Space vector PWM, THD, Grey wolf optimization.

Paper Id.: 42

Impact of high-k spacers on the switching and VTC characteristics of Gate-Stacked NCFET

Rashi Mann, Rishu Chaujar

Department of Applied Physics
Delhi Technological University, Delhi - 110042, INDIA

Abstract:

In this work, a Gate-Stacked Negative Capacitance Field Effect Transistor with a high dielectric material layer in the substrate region (GS-NCFET) is investigated. Also, the effect of different types of spacers is taken into account. Spacers are differentiated based on their dielectric constant i.e., GS-NCFET with no spacer is denoted as S0, with air spacer is denoted as S1, with SiO2 specified as S2, and with HfO2 noted as S3 device architecture. Further, the switching ratio (Ion/Ioff) is discussed for S0, S1, S2, and S3. It increases 750 times as we move from S0 to S3. Furthermore, the short channel effects (SCEs) like subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are extracted at drain-source voltage (Vds) of 0.5 V. SS is reduced by 14.58% in the linear region from S0 to S3, and DIBL is decreased by 41.17% as we move from S0 to S3. Moreover, transconductance (gm) and transconductance generation factor (TGF) are evaluated. Lastly, the voltage transfer characteristic (VTC) curve is considered for digital application purposes and the transition region is drawn out for all the device architectures.

Keywords: Negative capacitance, Gate-stacking, short channel effects, VTC curves.

Paper Id.: 43

Impact of temperature at atomic scale on DC and analog performance of Gate Stack GNRFET

Anshul, Rishu Chaujar
Department of Applied Physics
Delhi Technological University, Delhi –110042, INDIA

Abstract:

The scaling down in transistors causes a high leakage current and increases electron tunneling due to reduced channel length and gate oxide thickness. The gate oxide can be chosen from materials having a high dielectric constant to minimize the short-channel effects (SCEs) and leakage current. In this work, the performance of the gate stack graphene nanoribbon field effect transistor with gate stack (GS) architecture in dielectric layers using Quantum ATK simulator is studied. The semi-empirical (SE) calculator using the Slater-Koster model with NEGF formalism and without-self-consistent field (SCF) iteration method has been adopted to calculate the electronic properties for the conventional GNRFET and proposed GS-GNRFET device. The GS architecture improved the on current (Ion) by 30%, reduced the off current (Ioff) by 72%, increased the peak transconductance (gm) by 12%, and a better transmission spectrum is observed as compared with the conventional GNRFET. Additionally, the impact of various temperatures on the DC and analog performance of GS-GNRFET is studied. The rise in temperature from 250 K to 350 K reduces Ion by 48%, increases subthreshold swing (SS) by 56%, reduces switching ratio (Ion/Ioff) by 98%, and increases drain-induced-barrier-lowering (DIBL) by 138 times.

Keywords: Atomic scale simulation, Gate stack graphene nanoribbon field effect transistor, NEGF method, analog parameters.

Paper Id.: 44

Negative Capacitance FinFETs for low power applications: A Review

Ayushi Lamba, Rishu Chaujar
Department of Applied Physics
Delhi Technological University, Delhi – 110042, INDIA

Abstract:

The source-to-drain barrier of metal oxide semiconductor field-effect transistors (MOSFET), which is controlled by the gate voltage (VG), is the primary factor in determining the curent (I)-voltage (V) properties of MOSFETs. As per the Boltzmann statistics, in order to increase the current magnitude of a conventional MOSFET by an order, a gate voltage of atleast 60 mV must be applied. This 'Boltzmann tyranny' prohibits the present MOSFET's threshold voltage from dropping below 0.3V with a 5 decade Ion to Ioff ratio. The restriction on power dissipation in the contemporary Internet of Things era makes it obvious that a device with a reduced subthreshold swing would be an ideal option for well-ordered computation. Negative Capacitance FinFETs have become a hot topic of research in the present world as they have some potential benefits like ease of fabrication, process integration, ability to alter short channel effects (SCEs), and raised current driving ability due to reduced subthreshold swing. In this article the authors have attempted to thoroughly study the NC FinFET technology's current state-of-the-art which aims at enhancing device parameters like drain current, switching ratio, subthreshold swing and hysteresis. Additionally, comparative study of different NC FinFET structures for low power applications has been explored and summarised based on a number of criteria.

Keywords: Subthreshold swing, hysteresis, ferroelectric, NC FET, NC FinFET, low power application

Paper Id.: 45

Design and Analysis of Dual Source Vertical TFET with and without channel overlapped structure

Archana, Sheetal Singh, Subodh Wairya

Department of Electronics and Communication Engineering,
Institute of Engineering and Technology, Lucknow-226021, INDIA

Abstract:

This research paper emphasizes evaluating the structure and performance of a Dual Source Vertical Tunnel Field-Effect Transistor (DS-VTFET) at the device level. The investigation involves the analysis of two different DS-VTFET structures: one with a channel overlapped and the other without a channel overlapped. Introducing a channel overlap aims to boost the overall performance of the DSVTFET by improving specific device characteristics. The overlapped DS-VTFET demonstrates superior performance, including a high drive on current (ION = 1.20 × 10-4 A), reduced off-state current (IOFF = 3.95 × 10-14 A), and a sub-threshold slope (SS) of 11 (mV/decade), and average subthreshold swing (AVSS= 35.30 mV/decade), compared to the structure without overlap which has (ION =9.89 × 10-5 A, IOFF=2.96×10-13AVSS=12.77mV/decade, and AVSS=39.42mV/decade). These findings highlight the potential of the overlapped DS-VTFET for achieving improved performance in terms of current features and subthreshold performance.

Keywords: DS-VTFET, Subthreshold slope (SS), Average subthreshold swing (AVSS), Band- to- band tunneling (BTBT)

Paper Id: 47

Junctionless Accumulation Mode Surrounding Gate (JAM-SG) Hydrogen Gas

Shiv Shankar Yadav, Sachin Dhariwal, Sonam Rewari

Department of Electronics & Communication Engineering Delhi Technological University Delhi,India

Abstract:

In this paper, analysis of Junctionless Accumulation Mode Surrounding gate (JAM-SG) as a hydrogen gas detector has been done.JAM-SG with metal gate for gas sensing applications is proposed for the first time in this paper. A simulated model is developed for n-channel JAM-SG to observe the different electrical parameters of the device for different values of pressure [1]. Different simulated results such as surface potential, electric field and electron velocity have been analyzed at two different values of pressure10-14(Torr) and 10- 13 (Torr). At pressure10-14(Torr) work function of 5.0eV gets generated at metallic gate, maximum output drain current of 15.59µA at VDS=1V, the maximum output conductance of 145(µA/V) at VDS=0V and maximum transconductance of 7.7(µA/V) at VGS=0.8V is obtained, while at pressure of 10- 13 (Torr),work function of 5.2eV gets generated at metallic gate, maximum output drain current of 5.31µA at VDS=1V, the maximum output conductance of 61.2(µA/V) at VDS=0V, and the maximum transconductance of 8.45(µA/V) at VGS=1V is achieved.

Keywords: JAM-SG, hydrogen gas sensor, Surrounding Gate.

Paper Id.: 49

Dielectric-modulated Gate Engineered NCFET as a label-free biosensor

[1]Yash Pathak, [2]Anshul, [3]Bansi Dhar Malhotra, [4]Rishu Chaujar

[1, 2, 4]Department of Applied Physics, Delhi Technological University -110042, INDIA
[3] Department of Biotechnology, Delhi Technological University -110042, INDIA

Abstract:

This work observes the analog, electrical and switching parameter of double metal below negative capacitance FET (DM-B-NCFET). A cavitygap immobilization in dielectric modulation DM-B-NCFET has been proposed for many diseases. A comparative study of dielectric modulation has been taken with DM-B-NCFET immobilization various molecule such as protein, cholesterol oxide (ChOx), Streptavidin, without biomolecule. The analog impactof biomolecule on device has been studied like as enhanced transconductance for protein biomolecule, TGF, leakage current lower by 27.7%, lower subthreshold swing from without biomolecule. The observation has been shown in the form of electrical parameter as potential, electron concentration of all biomolecules. The dielectric constant is increased for improved characteristics of DM-B-NCFET device. The sensitivity of protein molecule is 7.7% higher than Streptavidin molecule. The biomolecule sensitivity is enhanced with progression of the dielectric constant. Cogenda visual TCAD simulator is applied for observing the result. The application of biomolecules is used to various analytes which have high speed, extreme density, low power consumption. The proposed device can detect particular biomolecule to diagnose various biomarker for disease like as lung and breast cancer.

Keywords: TCAD, Dielectric, NCFET, Ferroelectric material.

Paper Id: 50

Wearable MEMS Pressure Sensor with Temperature compensation for Diagnosing Neurological Disorders by Analyzing Spine configuration

[1]Sonali Biswas [2]Moushumi Biswas [3]Koushik Guha

[1]Jorhat Engineering College Assam Science and Technological University Jorhat, India
[2]Silchar Medical College and Hospital Srimanta Sankardev University of Health Science Silchar, India
[3]NIT Silchar Silchar Assam

Abstract:

MEMS Pressure sensors find wide applications in varied areas and it is a boon especially in Biomedical application. We know that there may be various changes in spine shape of an individual which depends upon the age group, the sleepware, the physical activity, acute injury, spine degeneration and postures in his day to day life. Any deviation in the spine shape from its natural erect position causes tension in the lower back muscles which leads to muscle fatigue and strain in a very short time. This abnormal spinal configuration may give rise to several neurological disorders. Diagnosis of the disorder is a must to arrest the problem from further degradation and proper medical intervention at the earliest. This paper proposes a High performance wearable piezoresistive pressure sensor which can measure the slightest deviation of the spine by measuring the strain developed in the lower back muscle. As piezoresistors are highly sensitive to temperature fluctuations a scheme is proposed for temperature compensation of this sensor. Any pressure above 20mm Hg may be responsible for several neurodegenerative diseases hence requires early diagnosis which can both alert and prevent one from several neurological disorders. The pressure sensing for minimum misalignment should be as low as 15mm of Hg or 1.59kPa to 30mm Hg or 10.6kPa which can cause ischemia or ulcer. The proposed sensor has range from 1kPa to 100kPa for early diagnosis of neurological disorders caused by spinal misalignment. The sensitivity is around 3.5mV/V/kPa.

Keywords: MEMS, Pressure sensor, wearable, strain, neurological

Paper Id.: 52

The Role of Log Power Monitoring Channel of BTRR and Strengthening its Input Signal by Installing a Line Driver between NLW-1000 and PA-1000

Md. Bodhroddoza Shohag, Md. Sayed Hossain, Md. Rakibul Hasan1, Md. Mobasher Ahmed1, Abdullah Al Mahmud, Md. Moazzem Hossain1, Mohammad Mezbah Uddin, Md. Abdul Malek Soner, Ashraful Haque, Nusrat Jahan
Center for Research Reactor, Bangladesh Atomic Energy Commission, Dhaka, Bangladesh
Kamrul Alam Khan
Department of Physics, Jagannath University, Dhaka, Bangladesh

Abstract:

Various experiments require very low reactor power to full power and for low power experiments, Wide-Range Log Power Channel (NLW-1000) plays a solely vital role. Therefore, it should be operational during rector operation as well as shutdown state and without the proper functioning of NLW-1000, it will be impossible to observe reactor power in a logarithmic scale as well as rector period. Suddenly, the NLW-1000 was not working properly, therefore, a new NLW-1000 and pre-amplifier (PA-1000) were installed. Then, the prestart checks showed that the "count rate low test" and the "count rate high test" were failed and this information indicates that there is a signal loose between the PA-1000 and the NLW-1000. To cope with this issue, a line driver was installed in the data transmission line between NLW-1000 and PA-1000 but again the prestart check showed the same result as before. Then, an oscilloscope is used to know the signal condition at different points in the total transmission line and the continuity checks of STP showed that the optocouplers in the FC-ISO-D and FC-ISO-C were inactive. By making a proper connection, the problem is resolved. After the system powered up, the voltage outputs at each point of the FC-ISO-D and FC-ISO-C as well as the outputs of the oscilloscope at different positions showed normal conditions. After all, the total prestart checks of NLW-1000 were passed. Various types of experiments are now going on using this BTRR facility by observing reactor power in a logarithmic scale as well as rector period.

Keywords: Power Monitoring Channel; Line Driver; Research Reactor; I&C System; Signal Boosting.

Paper Id.: 53

Power Efficient High Linear LNA for High-Efficiency WLAN Applications

V Thenmozhi, M. Bhaskar
Department of Electronics and Communication Engineering
National Institute of Technology, Tiruchirappalli – 620015, INDIA

Abstract:

This paper proposes a novel CG-CS-CS (CG-CS2) Low noise amplifier (LNA) with an external matching network for simultaneously improving the circuit's gain, power, and linearity performance to aid the WLAN applications. A CS with PMOS current source is cascaded with the conventional CG-CS amplifier to enhance the circuit linearity. This cascade structure is similar to the multi-gate transistor technique. In the proposed work, by adding the CS stage at the negative output, the noise figure (NF) of the proposed circuit is reduced by 0.53dB, and the IIP3 is improved by 6.435 dBm without consuming more power. This novel modified multi-gate structure is designed and implemented in Cadence UMC 65nm technology with a supply voltage of 1.2V. The proposed CG-CS2 LNA achieves a gain and NF of 16.21/19.1dB and 3.97/4.5dB, respectively, with (High linear mode)/without (High gain mode) the additional CS amplifier, which consumes only 3mW of power from the supply voltage. The designed single-differential-ended LNA operates at the frequency band 2.37-6.7GHz with S11 of <-10dB.

Keywords: LNA, CG-CS2, Modified multiple gate, High gain, High linear, NF, WLAN.

Paper Id.: 54

A Modular and Compact RF-MEMS Step Attenuator for Beamforming Applications Based on an Improved Coplanar Waveguide Structure

Girolamo Tagliapietra1, Jacopo Iannacci2, Koushik Guha3
1, 2 Center for Sensors and Devices (SD) Fondazione Bruno Kessler (FBK), 38123 Trento, ITALY
3 Department of Electronics and Communication Engineering, National Institute of Technology, 788010 Silchar,INDIA

Abstract:

The outstanding data rates supported by the 5th Generation (5G) network rely on the effective combination of high frequency bands, a widespread coverage offered by multiple kinds of small cells, and massive Multiple- Input-Multiple-Output antenna systems at the physical level. Characterized by hundreds of radiating elements, such antenna systems enable an extensive use of beamforming techniques to reach the desired goals in terms of throughput and suppression of interfering signals. Current hybrid (analog-digital) beamforming architectures are composed by a network featuring a huge number of attenuators and phase shifter, whose requirements, in terms of miniaturization, linearity and broadband behaviour, could be effectively addressed by means of Radio Frequency Micro-Electro Mechanical-Systems (RF-MEMS). In this work, starting from an arrangement of RF- MEMS step attenuator based on a modular approach, a novel design is presented and critically assessed. The resulting 4-bit compound relies on capacitive membranes and on an improved coplanar waveguide structure, targeting a better impedance matching along the considered 24.25-27.5 GHz interval. The simulated results demonstrated satisfying return loss curves along the entire 30 GHz span, and multiple states realizing the desiredattenuation levels. The reason behind the observed discrepancies between the expected and the achieved attenuation have been circumscribed and they will be addressed by ad hoc rounds of optimization.

Keywords: RF-MEMS, Beamforming, 5G, Attenuators, Step Attenuators.

Paper Id.: 55

Connecting the Unconnected: The Potential of 5G Satellite Convergence in Rural India

Rishabh Gupta, Ms. Sanchita Mallick
Department of Physics, Department of Electrical & Electronics Engineering, Adamas University, Kolkata,INDIA

Abstract:

The purpose of this paper is to give an overview of the integration of 5G mobile networks with NTN satellites to set up an infrastructure that can help the rural population. As the demand for faster and more dependable internetincreases, along with the pressure on network providers to serve a larger audience, it is also necessary to look at the underserved or areas with low populations where implementing a network infrastructure would be costly. Satellite-based internet backed by a 5G network can be beneficial in solving this issue. While it is not possible toimplement such a massive infrastructure all at once, the paper discusses the possible implementation by proposinga systematic model based on the proximity of the less populated areas with the highly populated areas, technologythat can help make this implementation possible, and lastly the user-end services, case studies, and future projectsand plans of implementing this technology.

Keywords: 5G, Non-Terrestrial Network (NTN), Rural connectivity, Satellites, Wireless communication.

Paper Id.: 56

Designing 8-bit Multiplier using Vedic Mathematics and Its Comparison with Conventional Multipliers

Nabajeet Sen Saurabh Chaudhury
Electrical Engineering Department National Institute of Technology Silchar Silchar, India

Abstract:

Vedic mathematics technique is faster and more accurate as compared to the conventional method of arriving at asolution to mathematical problem. The complexity of arithmetic procedures is reduced to a high level. So, if we use Vedic mathematics for the VLSI implementation of multipliers, the number of mathematical operations will reduce significantly. Thus, Vedic multipliers may be quite useful for applications like image processing, code compression etc. where the processing time will get reduced and the power consumption will also reduce significantly. Here we design and simulate an 8-bit multiplier using Vedic mathematics. Then we compare it with some conventional multipliers such as array multiplier, Booth's multiplier, Wallaces' multipler and found that for large multipliers it supersedes all other multipliers in terms of power, delay and area.

Keyword: Vedic Mathematics, Vedic Sutras, VlSI Implementation, Multiplier Algorithm.

Paper Id.: 60

A Survey on Physical Layer Security Techniques and Related Risk Management Frameworks for Cyber Secure Networks

Reshmi Begum[1], Sabyasachi Bhattacharyya[2] and Ehsan Sheybani[3]
[1] PCPS Girls' Polytechnic, Department of Computer Engineering, Guwahati, India
[2] PCPS Girls' Polytechnic, Department of Computer Engineering, Guwahati, India
[3] School of Information Systems and Management, University of South Florida

Abstract:

The data transmission in physical layer can occur upon physical medium and also through wireless medium such Wireless Sensor Networks. The concerns and measures taken in consideration regarding secured data transmission in the lowest layer of the Open System Interconnection model, termed as physical layer are called Physical Layer Security. To manage such security issues, it is important to know and understand the risks that can cause harm over the data and Risk Management Framework is a strategy, especially designed to deal with such situations in the information systems. This paper is a systematic literature review connecting cyber secure data communication over physical layer and cross layer security aspects associating them to RMF to help mitigate risks and threats for the data as well as users in mostly the physical layer.

Keywords: Wireless sensors networks, Mobile Networks, Open System Interconnection, Physical Layer Security, Risk Management Framework, Information systems

Paper Id.: 61

F AP bI3/hybrid CIGS-GeTe Optimized Tandem Solar Cell Design with Efficiency Beyond 43%

Arush Singh Koundal Ashwani Kumar Rana
Dept. of ECE NIT Hamirpur Hamirpur

Abstract:

This paper focuses on the optimisation of tandem solar cells by separately modelling and analysing the top and bottom subcells, then integrating them to create an efficient tandem cell structure. For the top subcell FAPbI3 is investigated, highlighting the significance of the absorber layer, HTL and ETL. For the bottom subcell hybrid CIGS-GeTe arrangement is analysed. The simulation of cell architectures and assessment of their performance characteristics are done using the SCAPS 1D tool. The investigation involves a look at how temperature and the thickness of the absorber layer affect the stability and effectiveness of the cell, giving significant information for refining the cell structure design. The proposed tandem structure yields high efficiency of 43.062%.

Keywords: Tandem Cells, Hole Transport Layer (HTL), Electron Transport Layer (ETL).

Paper Id.: 62

Enhancing Security in IoT Frameworks: A Comprehensive Review of Key Management Protocols and Authentication Mechanisms

Kirti Baliyan Dr. Priyanka Ahlawat
Dept. of Computer Engineering National Institute of Technology (Kurukshetra, Haryana) Kurukshetra, India

Abstract:

Wireless sensor networks face a significant challenge in handling unforeseen attack vulnerabilities, particularly in their self-declared safe algorithms. These vulnerabilities create potential entry points for adversaries to compromise the privacy of the network. Attackers can exploit weaknesses through aggressive or passive attack strategies, including passive eavesdropping and active tampering with sensitive information transmitted across the wireless sensor network. The perceptron layer, which constitutes a small portion of the Internet of Things (IoT) architecture, is found to be the primary target for attacks on wireless sensor networks and RFID tags. However, implementing robust security measures in IoT systems poses difficulties due to resource limitations in sensors, such as constrained memory, battery life, processing power, and bandwidth. To address these challenges, this research proposes the incorporation of lightweight triple DES (Data Encryption Standard) security strength into a password-based key agreement protocol. The objective is to establish a shared key for specific sessions, considering the three key goals of system configuration, user registration, and sensor registration via various gateways. By leveraging lightweight triple DES, the research aims to prevent the leakage of sensitive data and mitigate attacks like Man-inthe-Middle, sensor session key leakage, session hijacking, and data sniffing. The suggested technique employs concatenation and Exclusive OR operations to enhance the complexity of parameters and safeguard smartcard information in memory. The proposed approach ensures the security of the entire key generation phase. Through this study, fundamental issues in the authentication and mutual authentication stages of deploying wireless sensor networks in the Internet of Things are addressed, contributing to improved security and integrity within IoT systems.

Keywords: wireless sensor networks; IOT; physical attacks; cryptosystem; key generation;

Paper Id.: 63

CSI Feedback Compression for Massive MIMO System using Dilated Convolution and Complex Input Neural Network

Sikhamoni Das, Mrinmoy Sandilya, Aradhana Misra, Kandarpa Kumar Sarma
Department of Electronics and Communication Engineering, Gauhati University Guwahati, Assam, India

Abstract:

Massive Multiple Input Multiple Output (MIMO), is one of the core technologies of the next generation wireless communication. The performance of massive MIMO depends mainly on the accuracy of the downlink Channel State Infor-mation (CSI) available at the base station (BS). Existing CSI feedback algorithms for Frequency Division Duplexing (FDD) based MIMO systems mostly encounter the problem of low feedback accuracy and higher computational complexity. Hence, keeping these limitations in mind, a CSI compression based on Deep Learning (DL) for single-user and multi-user scenario and applicable to Massive MIMO systems has been developed and analysed in this paper. The work comprises of forming a new hybrid model with Complex Layer Input and Dilated Convolution, to effectively compress the CSI of a massive MIMO system. This hybrid model has been trained and tested using a dataset for outdoor scenario and the results obtained have been compared with the state-of-the-art models available.

Keywords: Massive MIMO, CSI feedback, deep learning, dilated convolutions. complex layer convolutional network.

Paper Id.: 64

A Compact 3 GHz Comparator for SAR-ADCs In Robotic Prosthetic Hand Designs

[1] Farhana Begum, [2] Md. Najrul Islam, [3] Kashif Akhtar Ahmedand, [4] Kandarpa Kumar Sarma

[1, 4] Department of Electronics and Communication Engineering, Gauhati University, Gauhati-781014
[2] School of Computing and Electrical Engineering, IIT Mandi, 175005
[3] Department of Orthopaedics, AIIMS Guwahati-781001

Abstract:

A compact low power and ultra-high-speed design of comparator is presented here. The conventional single tail comparator being replaced by the double tail comparator improves the sampling frequency at the same time reducing the power. The latch-based design at the evaluation node is seen to enhance the comparator operating performance by 30% and power dissipation by 70%. The simulation is carried out in a CADENCE virtuoso environment with GPDK 45-nm CMOS technology node.

Keywords: ADC, Prosthetic hand, Robotic hand, Delay, Sampling frequency, Dynamic power dissipation.

Paper Id.: 65

Design of a Blind-Aid spectacle for visually impaired people using Deep Learn algorithms and Face Recognition techniques

G T Guddla, R R Gowtham, B Santhosh, B N A Kumar, G U Kiran, Y M Jayanth

Mechanical Engineering Department, New Horizon College of Engineering, Bangalore, India,

Abstract:

Proper navigation and detailed perception are the vital needs of human life both in all environments. Eyesight protects human-beings from all kinds of dangers. Whereas, this is the major challenging task for visually impaired people. With emergent trends in day-to-day technology, many assistive tools have been developed like, braille compasses and white canes to help them. To further enhance the assisting aids of these people, the proposed system comes up with a Blind-Aid Spectacle with ultrasonic sensors for detecting obstacles and a stereo camera for capturing videos to perceive the surroundings, using deep learning algorithms and face recognition technologies. Visually impaired people can easily interact with the whole system via, a speech recognition module and all the information were stored in the cloud. The basic design of this Blind-Aid Spectacle was done with Fusion 360 software. This includes a fibre material design, where all the required components can be embedded in it including a head phone jack for voice assistant. The glass was made compact in size with water proof seal, so that it can be used in rain also.

Paper Id.: 67

Glomerulus-on-a-Chip, A Pathway for Future Kidney on Chip Technology: Challenges and Future Prospects

Bhagyashree Saud [(1)], Koushik Guha [(2)], Jasti Sateesh [(3)], Pratim Sengupta [(4)], Sergei Selishchev [(5)], Betiana Lerner [(6)], Maximiliano Sebastian Perez [(7)], K. Srinivasa Rao [(8)], Rajendra P. Shukla [(9)]

[(1)] Department of Electronics and Communication Engineering National Institute of Technology Silchar, Assam, INDIA,

[(2)] Department of Electronics and Communication Engineering National Institute of Technology Silchar, Assam, INDIA,

[(3)] Deptartment of Electronics and Communication Engineering VR Siddhartha Engineering College, Vijayawada, A.P., INDIA,

[(4)] Consultant Nephrologist and Transplant Physician Bellevue Clinic and ILS Group of Hospital, Kolkata, India

[(5)] National Research University of Electronic Technology (MIET) Building 1, Shokin Square, Zelenograd, Moscow, RUSSIA,

[(6)] Department of Electrical and Computer Engineering Buenos Aires 1706, Argentina, IREN Center, National Technological University, Florida, International University, Miami, FL 33174, USA,

[(7)] Biomedical Engineering Institute Buenos Aires University, Buenos Aires C1063ACV, Argentina, Collaborative Research Institute Intelligent Oncology (CRIION), Hermann-Herder- Straße 4, 79104 Freiburg im Breisgau, Germany,

[(8)] Professor & Head of Microelectronics Research Group Department of ECE KL University,Green Fields, Vaddeswaram, Gunter-Dist, Andhra Pradesh, INDIA

[(9)] BIOS Lab-on-a-Chip Group, MESA+ Institute for Nanotechnology Max Planck Center for Complex Fluid Dynamics, University of Twente, P.O. Box 217, 7500 AE Enschede, The

Abstract:

Glomerulus-on-a-chip (GoC) is an innovative in vitro organ model which is a recent advancement in the field of microfluidic-based organ-on-a-chip research. GoC is basically used to study glomerulopathy, test drug nephrotoxicity and to imitate the functions of filtering membrane in the glomerulus. As part of the glomerulus-on-a-chip, a microfluidic device is used to co-culture podocytes and endothelial cells and physical stimulation is used to enhance cell function so that a functional filtration barrier can be constructed. The functional barrier can be assessed by permeability experiments utilizing molecules with fluorescent labels, such as albumin and inulin. The glomerulus-on-a chip technology in conjunction with the cell culture technology could potentially eliminate the need for animal testing by offering an alternate organ model. This review paper provides an overview of the characteristics of the current glomerulus-on-a-chip systems, with an emphasis on challenges involved in selective permeability verification tests. Finally, we discuss the possible future approaches that should be created to address those issues and enable further glomerulus-on-a-chip technology progress.

Keywords: Glomerulus-on-a-Chip, podocyte, organ-on-a-chip microfluidic device.

Paper Id.: 68

Modelling of Dielectric Pocket-Engineered Dual Metal Nanowire Ferroelectric MOSFET (DPE-DM-NW-Fe FET) to minimize Gate Induced Drain Leakages (GIDL)

Shalu Garg[1], Jasdeep Kaur[2], Anubha Goel[3], Subhasis Haldar[4] and R.S. Gupta[5], Life Senior Member, IEEE

[1, 2] Department of Electronics and Communication Engineering, Indira Gandhi Delhi Technical University for Women, Kashmere gate, New Delhi, India.
[3, 5] Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, New Delhi, India.
[4] Department of Physics, Motilal Nehru College University of Delhi, New Delhi, India.

Abstract:

In this research article, the simulation study on dielectric pocket engineered dual metal nanowire ferroelectric (DPE-DM-NW-Fe FET) has been proposed to reduce GIDL in the off state and also lower the sub-threshold swing. GIDL is an unenviable phenomenon that occurs even when gate voltage is almost zero. When the gate region is placed at a lesser bias and the drain region is placed at a greater bias, it becomes significant. As a result, the channel potential difference rises, signifying the release of minority carriers that tunnel across the gate oxide and result in gate leakages in the form of GIDL current. The dielectric pockets introduce a diffusion stopper that serves as an insulating barrier and prevents the off-state current. So, the simulation is carried out to analyze off-state GIDL currents of DPE-DM-NW-Fe FET. The simulations have been conducted on various channel lengths (=30nm, 40nm and 50nm). It has been thus observed that GIDL current reduces to an order of 10 µA. Owing to the presence of ferroelectric layer; the value of subthreshold swing has been reduced below 60 mV/decade (Boltzmann tyranny). Internal voltage amplification has been inherited in the device due to presence of negative capacitance phenomenon. The following parameters have been modelled for different contemplated channel lengths: electric-field, electron- concentration, electron-velocity, and surface potential. In terms of drain-current, trans-conductance (gm), and output-conductance (gd), it has been observed that the DPE-DM-NW-Fe FET exhibits excellent performance. DPE-DM-NW-Fe FET can thus be implemented for high frequency applications. For simulations, ATLAS 3-D device simulator has been used.

Keywords: Dual metal gate, ferroelectric material, negative capacitance phenomenon, transconductance, output transconductance, GIDL.

Paper Id.: 70

Impact of Interface Trap Charges on Noise and Electrical Properties of 4H-SiC Based Gate-Stack, Dual Metal,Surrounding Gate, FET(4H-SiC-GSDM-SGFET)

Neeraj[1], Shobha Sharma[2], Anubha Goel[3], Sonam Rewari[4], S.S Deswal[5] and R.S. Gupta[6], Life Senior Member, IEEE

[1, 2] Department of Electronics and Communication Engineering Indira Gandhi Delhi Technical University for Women, Kashmere gate, New Delhi, India.
[3, 5, 6] Department of Electronics and Communication Engineering Maharaja Agrasen Institute of Technology, New Delhi, India.
[4] Department of Electronics, Delhi Technological University, New Delhi, India.

Abstract:

This article investigates the impact of various interface trap-charges on noise & electrical characteristics for Silicon Carbide Based Gate – Stack, Dual Metal, Surrounding Gate, FET (4H-SiC-GSDM-SGFET) & Silicon Carbide (4H-SiC) Based Dual Metal, Surrounding Gate, FET (4H-SiC-DM-SGFET). For both the devices, output characteristics including transconductance (gm), output conductance (gd), drain current (Ids), gate capacitance (Cgg) and cutoff frequency (fT) have been examined. Superior characteristics have been observed for the proposed device. Additionally, it has been investigated how charge-traps affects noise figure (NF). Proposed structure has been found to have a lower NF, making it more noise-resistant.

Keywords: Dual metal; Gate- stack; 4H-SiC; Interface charge traps; SCE.

Paper Id.: 71

A Systematic Literature Survey on Evolutionary Computational Techniques for 5G and Future Generation 6G Networks

Shruti Bhowmick, Simashree Das, Pronamee Konwar Amisha Bodo, Sabyasachi Bhattacharyya
PCPS GIRLS' POLYTECHNIC, Computer Engineering Department, Guwahati- 781021

Abstract:

Necessary steps taken towards expanding the 5G network is by promoting native innovation. With the introductionof 5G technology, the world is also trying to introduce 6G with better technology and it is assumed that the 6G network is 100 times faster than the current 5G network. Recent research in this field of study is investigating the potential of computational offloading in 6G network. In this paper a systematic survey have been done regarding the future computational benefits of 5G future successor.

Keywords: Computational offloading, 5G, Edge computing, Cloud computing, Successor, Fog computing, 6G, Quantum computing

Paper Id.: 72

Analysis of Silicon Carbide as a Membrane for CMUT with its Different Radius Effect

F. Lalmalsawmzuali, Reshmi Maity, Niladri Pratap Maity*

Department of Electronics & Communication Engineering, Mizoram University (A Central University), Aizawl-796004, INDIA

Abstract:

Capacitive Micromachine Ultrasonic transducer (CMUT) has emerged as a substitute to conformist piezoelectric transducer. They offer many advantage in terms of bandwidth, sensitivity and efficiency. This paper presents the analytical model of electrostatic force generated with capacitance action, the effect of membrane radius in capacitance and the enhancement of electrostatic force with inclusion of fringing effect. A membrane of SiC and $Si3N4$ with varying radius i.e., 12.5μm, 28μm, 43μm, 50 μm, 53 μm is analysed. Simulation of 12.5μm SiC membrane radius is carried out in COMSOL Multiphysics.

Keywords: CMUT, Ultrasonic, SiC Membrane, COMSOL Multiphysics

Paper Id.: 73

Investigation of Capacitive Micromachined Ultrasonic Transducer Based on the Membrane Materials

H. Lalnunfeli[1, 2], Reshmi Maity[1], Ramesh Chandra Tiwari[2], Niladri Pratap Maity[1]
[1]Department of Electronics and Communication Engineering,
[2]Department of Physics,
Mizoram University (A Central University), Aizawl-796004, INDIA

Abstract:

Using COMSOL Multiphysics, 3-D Capacitive Micromachined Ultrasonic Transducer (CMUT) is modelled and investigation is done using three different materials; Silicon Nitride (Si3N4), Silicon Carbide (SiC) and Diamond as the membrane material. Observations are done using different parameters of the proposed CMUT model to see the best material for the membrane by comparing in the resultant frequency, displacement, capacitance and polarization shown by using the three mentioned materials. From the observations, the usage of silicon nitride as membrane material consequences to be a perfect material as the best characteristics of our CMUT model are obtained by the use of it for the membrane material.

Keywords: CMUT, MEMS, COMSOL Multiphysics, Ultrasonic Sensors

Paper Id.: 74

Analysis of a Low frequency MEMS Capacitive Accelerometer under the effect of Biasing Voltage for detection of Parkinsons Tremor

Preeti M[1,2], Koushik Guha[1], K L Baishnab[1], Jacopo Iannacci[3], Massimo Donelli[4], Narayan Krishnaswamy[5]

[1]Electronics and Communication Engineering Department, National Institute of Technology, Silchar, Assam
[2]Department of Electronics and Communication Engineering, Koneru Lakshamaiah Education Foundation, A.P, India
[3]Centre for Sensors and Devices (SD), Fondazione Bruno Kessler (FBK), Trento,Italy
[4]Department of Civil, Environmental and Mechanical Engineering (DICAM), University of Trento, Trento, Italy.
[5]Department of AI & ML, Nitte Meenakshi Institute of Technology, Bengaluru, Karnataka, INDIA

Abstract:

The paper presents a comprehensive analysis of the design and simulation of a MEMS differential capacitive accelerometer optimized for the detection of tremor signals in Parkinson's disease patients. The accelerometer design aims to address the sensing challenges at very low frequencies (<10 Hz) associated with Parkinson's tremors, specifically targeting the frequency range of 3.5-7.5 Hz. The design process considers various parameters to optimize the resonant frequency, mechanical stability, and sensitivity of the accelerometer. Finite element analysis (FEA) using COMSOL Multiphysics validates the design approach, demonstrating a resonant frequency of 5.5 Hz with a maximum displacement of 1.77 μm at an acceleration of 0.04 g at a biasing voltage of 10 V. This proposed design exhibits a noteworthy mechanical sensitivity of 44.25 μm and an electrical sensitivity of 1.428 nF/g, emphasizing its capacity to detect and respond to minute physical and electrical changes with high precision. Analytical models are developed to calculate the resonant frequency and effective spring constant, which further characterizes the accelerometer's mechanical behavior. The proposed design achieves a comparable dynamic range, high sensitivity, linear response, and minimal cross sensitivity when compared with existing literature. The proposed MEMS differential capacitive accelerometer exhibits significant potential for precise measurement and quantification of tremor signals in individuals afflicted with Parkinson's disease. By accurately capturing and analyzing these tremor signals, this accelerometer has the capacity to contribute significantly to the advancement of medical diagnosis and monitoring in the field of Parkinson's disease.

Keywords: MEMS, Sensor, Finite Element Analysis, Parkinsons Disease, Low frequency.

Paper Id.: 75

Survey on Implementation of Turbo Encoder & Decoder using FPGA

Sampath babu, Ganesh, Bhuvan, Mrudula
Electronics and communication engineering
Velagapudi Ramakrishna Siddhartha Engineering College, Vijayawada-52007, INDIA

Abstract:

Turbo codes are efficient and powerful error correction techniques used in modern communication systems. The turbo encoder and decoder are key components of such systems. In this survey paper, we explore the implementation of a turbo encoder and decoder using field programmable gate arrays (FPGAs). Specifically, we focus on the implementation of the turbo decoder using the Viterbi algorithm. The Viterbi algorithm is a dynamic programming algorithm that finds the most likely sequence of states in a finite-state machine. The turbo decoder uses the Viterbi algorithm to decode the soft output from the turbo encoder. The implementation of the turbo decoder using the Viterbi algorithm on an FPGA allows for high-speed and low-latency decoding, which is essential for real-time communication systems. We discuss the various approaches to implementing turbo codes on FPGAs, including parallel concatenation of convolutional codes, recursive systematic convolutional codes, and serial concatenation of convolutional codes. We also review the performance of the turbo codes implemented on FPGAs, such as throughput, latency, and error rate.

Keywords: FPGA, turbo encoder, turbo decoder, state diagram, RSC, interleaver, Viterbi algorithm.

Paper Id.: 76

A Social Welfare Optimization Algorithm for Efficient Incorporation of Demand Response in Modern Power Grids

Suparna Maity, Sandip Chanda, Papun Biswas, Abhinandan De
Electrical Engineering Department Global Institute of Management & Technology, Nadia, India Ghani Khan Choudhury Institute of Engineering and Technology, Malda, India JIS College of Engineering, Kalyani, India Indian Institute of Engineering Science and Technology (IIEST), Shibpur, Howrah,

Abstract:

Worldwide power grids by changing their policy and also infrastructure and it is enhancing Smart day by day consecutively support Renewable Energy Sources (RES). This Smart Grid is contributing new resources such as Demand Response (DR) which can be utilized for continuous grid operation of the existence of RES. Demand side management through demand response however only electricity price based and optimised schedule based only on the same strategy may enforce such schedule of generators(GENCOs) and load dispatch centers (LDCs) and DISCOs that may not be sustainable in terms of deviation of powerful system parameters such as power factor, congestion of transmission line, voltage, reliability and stability of electricity supply. To detect this problem the proposes of work of optimisation framework, model and algorithm with an objective of security constraint social welfare optimisation to use the DR resource optimally for the profit of all the power demand players with no limit violation. The algorithm uses artificially intelligent DEQ Particle Swarm Optimisation (DEQPSO) owing to the high nonlinearity and complication of the objective function. Here proposed algorithm was tested in a modified IEEE 30 bus system and demonstrated to produce encouraging results. All simulations are performed through MATLAB 2018a.

Keywords: Renewable Energy Sources (RES), Smart Grid, optimisation framework, social welfare, Demand Response (DR) programme, DEQPSO.

Paper Id.: 78

An Inductive power transfer-based DC-DC converter with reduced voltage stress across switches

Anamika Das [1*], Ananyo Bhattacharya[2], Pradip Kumar Sadhu[3]
[1,2] Electrical Engineering Department, NIT Jamshedpur, Jharkhand, India.
[3] Electrical Engineering Department, IIT(ISM) Dhanbad, Jharkhand, India.

Abstract:

This article describes the integration of a Class-Ø2 inverter and a class-E/F3 rectifier applied in an inductively coupled power transfer (IPT) system. Class-Ø2 resonant inverters have the ability to reduce switch voltage stress and implement ZVS. A class E/F3 resonant rectifier is used in the receiving side of the wireless power transfer (WPT) system, which can reduce the peak voltage stress on the diode. This system is then optimized for maximum transmission efficiency. PSIM simulations of the proposed class ø2-E/F3 combined WPT system at 50 kHz showed a dc-dc efficiency of 94.56 percent.

Keywords: Wireless power transfer (WPT), zero-voltage switching (ZVS), zero-derivative voltage switching (ZDS), Resonant ClassØ2 inverter, Class E/F3 rectifier. PSIM.

Paper Id.: 79

Crop Yield prediction in West Bengal using Machine Learning Algorithms in MATLAB

Uttiyo Das Sarma, Saptadeep Choudhury, Debjit Debnath, Ms. Sanchita Mallick, Dr. Tirtha Majumder
Electronics and Communication Engineering Adamas University, Kolkata -700126, INDIA

Abstract:

Agriculture has been a vital in India since primeval times. Here the basic material from which a product is made obtained from agriculture for all primary industries like cotton, sugarcane, etc. Aside from this, many other industries indirectly depend on agriculture, such as rice mills, wheat mills and so on, which require raw materials. However, despite increasing industrialization, employment in the agriculture sector is not decreasing, there are new opportunities. Meanwhile, farmers also face the problem in understanding which crop needs to be grown at what season of the year. We have chosen West Bengal because of its density of livelihood depending predominantly on agriculture which made it known as an agrarian State. It sustains roughly 8% of India's population and makes up 2.7% of its geological area. There are 71.23 lakh agricultural households, 96% of which are small and marginal farmers, according to studies. 0.77 hectares is the typical area of land occupation. West Bengal, however, is blessed with a variety of natural resources and agroclimatic conditions that enable the production of a wide variety of crops. Here we have used Machine Learning algorithms to find the method with highest accuracy and used it further to predict future production. A trained model has been run through and compared with a datasheet of similar format to calculate the yield of crop. Additionally, comparisons between three least count methods are made, and the best environment and model for this research are identified through analysis of the results. Advancement of the work will be able to calculate larger domain of crops in various parts of India. Also, the accuracy of the model will be more precise. [1][2]

Keywords: RMSE, R-square, MSE, MAE, Regression Learner, Ensemble Bagged Tree.

Paper Id.: 80

Analysis and performance improvement of AlGaAs/GaAs hetero-junction pin solar cell through optimization of active absorption layer

Pramita Nath and Abhijit Biswas
Department of Radio Physics and Electronics, University of Calcutta, 92 Acharya Prafulla Chandra Road, Kolkata-700009, India

Abstract:

In this work, we investigate the photovoltaic performance of p+-Al0.8Ga0.2As/p-GaAs/i-GaAs/n-GaAs/ n+-Al0.8Ga0.2As based multi-junction solar cell by varying the intrinsic layer thickness ranging from 0.04-0.1 µm and shallow layer thickness in the range 0.6-1.8 µm in terms of open circuit voltage (Voc), short circuit current density (Jsc), fill-factor (FF), and power conversion efficiency (PCE) at AM1.5G solar spectrum. Our optimised solar cell featuring intrinsic layer thickness of 0.06 µm and shallow doped region width of 1.2 µm offers Voc of 1.043 V, Jsc of 27.11 mA.cm-2, FF of 0.88, and PCE of 25%, respectively. Importantly, the proposed device shows excellent photo-voltaic performance in terms of PCE as high as 32.8% as compared to that of the conventional solar cell.

Keywords: AlGaAs/GaAs PIN solar cell, heterojunction, shallow doped layer, PCE.

Paper Id.: 81

A Review of Wireless Communication Technologies for applications in Smart Metering

Md Atiqur Rahman and Jayanti Choudhary
Department of Electrical Engineering,
National Institute of Technology Patna, Patna - 800005, Bihar, India

Abstract:

With the advancement in automation and smart systems, many problems that occur due to human error and inefficiency has been reduced prominently in different fields. In the field of power system, smart metering is a revolution to overcome problems of human inefficiency and to create awareness for consumers about their energy usage. It is possible due to Internet of Things technology under industrial revolution 4.0. This paper addresses the various aspects of different wireless communication technologies utilized in the IoT integration of smart meters and analysed the performance of these technologies on the parameters which is essential for smart metering application. In the country like India, where most of the populations are living in the rural areas and the network connectivity is still a big challenge. The installation of smart meters in various household is still in progress and various communication technologies have been used for the integration in smart meters but still we are facing many issues which are discussed in this paper. Although there are numerous review papers on wireless communication technologies, none of them have specifically addressed how to incorporate these technologies into applications for smart meters. Based on the issues and challenges associated with existing smart meters, a detailed analysis of wireless communication technologies on multiple aspects which are essential for the integration of communication technologies are discussed in this paper which can be helpful for the researchers and companies working in this area.

Keywords: Smart Energy Meter, Internet of Things (IoT), Wireless Communication Technologies, LoRaWAN

Paper Id.: 84

Flicker Noise Assessment of HDDP-DG-NCFET in Presence of Interface Traps and Temperature

Malvika*[1] (Corresponding author), Jagritee Talukdar [2], Bijit Choudhuri [1], Kavicharan Mummaneni [1]
[1] Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India
[2] Department of Electrical Engineering, Indian Institute of Technology Bombay, Maharashtra, India

Abstract:

The impact of noise on the functionality of nanoscale geometries is significant when it concerns the reliability of semiconductor devices. At lower frequencies, flicker noise dominates and affects various performance metrics of the device. This paper explores the analysis of flicker noise of highly doped double pocket double gate NCFET (HDDP-DG-NCFET) in the existence and non-existence of interface trap charges. The influence of the Gaussian donor type of interfacial trap charges (ITC) at the silicon/oxide boundary has been taken into account. Furthermore, the impact of temperature fluctuations (200K-400K) are considered for various noise parameters such as gate voltage and drain current noise power spectral density (Svg and Sid). It has been observed that, at lower temperatures the existence of ITC adversely affects the noise power spectral densities. However, as temperature rises, the influence of ITC becomes insignificant, but noise performance deteriorates significantly.

Keywords: HDDP-DG-NCFET, Trap charges, Temperature, Flicker noise, Noise power spectral density

Paper Id.: 86

Nano-biomolecule Identification Using Superlattice AlGaN/GaN High-K MOSHEMT: A Cutting-Edge Biosensing Technique

Tulip Kumar Saha[1,2], Moumita Mukherjee[3, *] and Rudra Sankar Dhar[1]
[1, 2] Department of Electronics and Communication Engineering,
[1] National Institute of Technology Mizoram, Aizawl 796012, India
[2] School of Engineering and Technology, Adamas University, Kolkata, West Bengal, India
[3] Department of Physics, School of Basic and Applied Sciences, Adamas University, Kolkata, West Bengal, India

Abstract:

This paper reports biomolecule identification process using a novel biosensing technique with high-K metal-oxide-semiconductor high electron mobility transistor (MOSHEMT). The authors have developed a MOSHEMT device with high-K dielectric material to improve the sensitivity of biosensors. High-K dielectric material is utilized to examine the electrical efficacy of MOSHEMT-based biosensors. When high-K materials are utilized, Two-Dimensional Electron Gas (2DEG) benefits from carrier confinement and leakage current reduction. Therefore, the on-current of the device has been increased. For numerical modeling, TCAD Silvaco Atlas is used. For label-free identification of biomolecules, simulation is used to investigate and compare various performance factors with SiO2 MOSHEMT. Experimental evidence verifies the accuracy of the model. According to the authors' knowledge, this is the first investigation on high-K dielectric AlGaN/GaN MOSHEMT biosensors for efficient label-free biomolecule detection. AlGaN/GaN MOSHEMTs, which use a high-K material, are promising features for use in biosensors.

Keywords: Biosensor, 2DEG, high-K dielectric, threshold voltage, sensitivity, label free detection.

Paper Id.: 87

Sensing of various kinds of biomolecules using hetero-structured tunnel FET in wet and dry environments

[1] Prarthana Chakraborti, [2] Abhijit Biswas, [3] Abhijit Mallik
[1,2] Department of Radio Physics and Electronics University of Calcutta, A. P. C. Road, Kolkata, West Bengal, INDIA
[3] Department of Electronic Science University of Calcutta, A. P. C. Road, Kolkata, West Bengal, INDIA

Abstract:

This paper investigates the detection of a wide variety of neutral biomolecules characterised by their corresponding dielectric constants ranging from low-K to high-K using Tunnel FET featuring hetero-structure source consisting of germanium and Si0.7Ge0.3. The detection and sensing analysis are performed in both wet and dry environments. Well calibrated SILVACO ATLAS device simulator is used to obtain device transfer characteristics that are exploited to compute the detection sensitivity. The variation of sensitivity is investigated with the dielectric constant of biomolecules, and a comparative analysis is presented for dry and wet conditions. The maximum sensitivity of 1.32 V is obtained in Wet environment condition by using the proposed structure which is higher or comparable to earlier reported data.

Paper Id.: 89

Overview on New Era Beyond MOSFET for High Speed and Computational Properties

Rituraj[1], Mukesh Kumar[1], S. Nandi[1], S. K. Dubey[2], M. Pandey[1] and A. Islam[1]
[1, 2] Dept. of ECE
[1] BIT, Mesra, Ranchi, Jharkhand, India
[2] G. Pullaiah College of Engineering and Technology, Kurnool, Andhra Pradesh, India

Abstract:

Conventional Metal-Oxide-Semiconductor FET (MOSFET) technology has been the industry standard in the electronics domain over the last four decades. In this time, MOSFET design has been rigorously optimized with gate length (LG) scaled down from over 10 µm in 1970s to 20 nm in the year 2014 (later, industry giant TSMC started 16 nm FinFET technology from the year 2015 and now it has reached 5 nm FinFET technology and is planning for 3 nm in near future). MOSFET miniaturization enables higher packing density, integration capabilities, improved performance due to reduced parasitic capacitances and resistances, enhanced switching speeds and lower power consumption, enabling the realization of advanced integrated circuits with increased functionality and improved overall system performance. As the size of MOSFETs approach that of a few silicon atoms, we experience fundamental physical and technological constraints, such as quantum tunnelling, leakage currents, and process variations, which hinder further size reduction as per Moore's law. To exploit mature silicon-based fabrication technology, an effort must be made to integrate emerging CMOS technologies with existing fabrication techniques. In our work, we review nanowire FETs, carbon nanotube FETs, graphene FETs and other emerging technology with high speed, performance and computational properties.

Keywords: Nanodevice; MOSFET; CMOS; CNT; Graphene; Nanoribbon; Nanowire

Paper Id.: 91

Improvement of Power Quality in Microgrid Connected Renewable Energy System Using Hybrid SMO_GEO Tuned STATCOM.

Amit Kumar[1*] Jayanti Choudhary[2]
[1*] Research Scholar, Department of Electrical Engineering, NIT Patna, India
[2] Assistant Professor, Department of Electrical Engineering, NIT Patna, India

Abstract:

Now a day's power generation from HRES like PV, FC, and Battery are subject to weather conditions, which can result in power quality (PQ) problems such voltage variations, harmonics, swells, and sags. To compensate for these PQ issues, a STATCOM can be used for reactive power compensation. In This work, proposes a model that integrates a STATCOM with an HRES to enhance the system's fixed operating limit and compensate for PQ issues. The proposed model uses an optimized Cuk-SEPIC converter to improve voltage regulation and reduce output voltage ripple, and hybrid optimization techniques such as Golden Eagle Optimization (GEO) and Slime Mould Optimization (SMO) are used to optimize the STATCOM parameters for maximum efficiency.

Keywords: Power Quality (PQ), Synchronous Compensator (STATCOM), Single-Ended Primary-Inductance Converter (SEPIC), Golden Eagle optimization (GEO), Slime Mould optimization (SMO).

Paper Id.: 92

Design of Morse Message Transmission and Reception using LASER

Syed Ashruf, Karumuri Srinivasa Rao, Girija Sravani Kondavitee
Microelectronics & VLSI Research Group, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Andhra Pradesh, India.

Abstract:

In this paper, we have implemented Morse code transmission using an Arduino and a laser. The Arduino board is used to control the transmission process, while the laser serves as the light source for emitting the Morse code signals. The Arduino is programmed to generate the appropriate patterns of dots and dashes based on the input text. Each character is converted into its corresponding Morse code sequence, and the Arduino controls the laser to emit short flashes for dots and long flashes for dashes. By combining the Arduino's control capabilities and the laser's light emission, we can effectively transmit Morse code messages. This paper provides a practical and hands on approach to learning about Morse code communication while utilizing the Arduino platform for control and the laser for optical signal transmission.

Keywords: Morse code, Transmitter, Receiver, Laser, Optical communication, Communication system, Information transmission, Photodetector.

Paper Id.: 94

A Simple Approach of Optical Fiber-Based Sensor for Liquid Turbidity Measurement

Sangeeta Das[1], Papiya Dhara[1*], Soumen Ash[2, †], Vinod Kumar Singh[2], Indranil Dutta[1]
[1] Department of Physics, Adamas University-Kolkata 700126, INDIA
[2] Indian Institute of Technology (Indian School of Mines) Dhanbad 826004, INDIA
[†]Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden, 01069 Dresden

Abstract:

The paper deals with a systematic study of optical fiber based turbidity sensor. Intensity modulated sensing mechanism has been incorporated and determination of sensitivity has been confided on output signal sustain some loss. Three different mediums, such as, glucose mixed with water, milk mixed with water, soil mixed with water have been used as sample. Beer-Lambert law has been implemented to study the transmittance and absorbance of the light while passing through different concentration of liquid sample. The output power range, sensitivity and resolution of the reported sensor have been achieved as 1.82 μW, 0.091 μW/NTU and 0.109 NTU respectively. Various future prospects of the basic experimental set-up have been estimated, specially using its sensing features for detection of liquid food quality. Finally, a blueprint of fiber optics turbidimeter has been presented with simple, repeatable measurement technique.

Keywords: Optical fiber sensor, Turbidity sensor, Intensity modulated sensor, Optical sensor, Water quality and health

Paper Id.: 95

Sensitivity Analysis of a Label-Free Detection Biosensor Utilizing Dielectric-Modulated Tunnel-FET.

Syed Ashruf[*1], Velisala Prudhvi Gopal[1], Md. Bismil[1], K. Girija Sravani[2], K Srinivasa Rao[2]
[1] Research Scholar, Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India
[2] Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India

Abstract:

In this research study, we have developed and simulated a novel configuration of a Dielectrically Modulated Double Gate Tunnel Field-Effect Transistor (DM-DG TFET) integrated with dual nanocavities. Our primary aim was to explore the potential of this device as a label-free biosensor for detecting biomolecules. The Silvaco Atlas model was utilized to analyze the electrical properties of the DM-DG TFET when exposed to various biomolecules. We evaluated several crucial sensing parameters, including current, threshold voltage, and subthreshold slope, for each biomolecule. Additionally, we extensively investigated the filling factor parameter associated with the nanocavity in our proposed device. Through our comprehensive investigation, we have gained valuable insights into the performance characteristics of the DM-DG TFET biosensor and its intricate interaction with biomolecules derived from cancer cells.

Keywords: Dielectrically Modulated Double Gate Tunnel Field-Effect Transistor (DM-DG TFET), Dual nanocavities, Label-free biosensor, Silvaco Atlas model.

Paper Id.: 96

A Comparative Study of L-Shaped Tunnelling Field Effect Transistor and Fully Depleted Metal Oxide Semiconductor Field Effect Transistor

Velisala Prudhvi Gopal[1*], Korivi Akhil[1], Md. Bismil[1], K Srinivasa Rao[2], K. Girija Sravani[2] [1]Research Scholar, Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India
[2]Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India

Abstract:

This study introduces a novel L-shaped Tunnel FieldEffect Transistor (LTFET) incorporating BOX (Buried oxide) for the purpose of low-power applications. The primary aim of this study is to examine the performance parameters, particularly focusing on stability, of the proposed LTFET design, while intentionally disregarding the fabrication process. The LTFET, featuring an L-shaped architecture, demonstrates enhanced stability, short channel effects (SCE's), and heavy ion irradiation specifically tailored for low-power scenarios, surpassing previous designs. Significant improvements are observed in both the ON-state and OFF-state currents. A thorough comparative analysis is carried out to compare the LTFET with the Fully Depleted Silicon-on-Insulator (FDSOI) MOSFET, focusing on various performance aspects such as drain current, potential, electric field, and energy band characteristics. This analysis reveals a notable decrease in subthreshold swing and threshold voltage for the L-shaped TFET compared to the FDSOI MOSFET. Additionally, the performance parameters of the LTFET exhibit a relative superiority over the FDSOI MOSFET, as substantiated by the comparative analysis. This research contributes to the advancement of low-power electronic devices by introducing a promising L-shaped TFET design that embodies improved stability and performance parameters [31]. The findings presented here offer valuable insights for future research and development in the field of low-power electronics
Keywords: LTFET, comparative analysis, subthreshold swing, threshold voltage, drain current.

Paper Id.: 97

Design and Analysis of Double-Gate p-n-i-n Tunnel Field Effect Transistor

Korivi Akhil[1*], Syed Ashruf[1], Md. Bismil[1], K Srinivasa Rao[2], K. Girija Sravani[2]
[1] Research Scholar, Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India
[2] Microelectronics & VLSI Research Division, Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation (Deemed to be University), Green Fields, Vaddeswaram, Guntur, A.P, India

Abstract:

This research study focuses on examining the influence of incorporating a narrow n-layer within the tunnelling junction of the p-i-n Tunnelling Field-Effect Transistor (TFET) as a potential solution to enhance device reliability in the presence of intense electric fields. Utilizing technology computer-aided design simulations, the effectiveness of this modification in transforming the device into a p-n-i-n TFET is demonstrated. Results show not only an improvement in the drive current, consistent with previous findings, but also an overall enhancement in reliability. A comparative analysis with the conventional p-i-n TFET highlights several advantageous properties of the p-n-i-n TFET, including higher ON-current, reduced, improved lower OFF-current, and higher drain current.

Keywords: p-i-n Tunnelling field-effect transistor (TFET), p-n-i-n tunnelling field-effect transistor (TFET), Reliability enhancement, Quantum tunnelling, Low power operation, High switching speeds, Performance improvement

Paper Id.: 98

Adsorption-based Microsensors for Protein Detection: Influence of Protein Structural Transformations and Adsorption-induced Depletion of the Analyzed Sample on the Sensor Noise

Ivana Jokić[1], Olga Jakšić[1], Miloš Frantlović[1], Zoran Jakšić[1], Koushik Guha[2]
[1] University of Belgrade - Institute of Chemistry, Technology and Metallurgy – National Institute of the Republic of Serbia, 11000 Belgrade, Serbia
[2] National MEMS Design Centre, Department of Electronics and Communication Engineering National Institute of Technology, Silchar, Assam, India

Abstract:

The noise originating from the random nature of processes that affect the time evolution of the number of adsorbed molecules is inherent to adsorption-based biosensors. It is a fundamental noise, so it determines the ultimate detection limit of such sensors. In this paper we develop a noise model of protein microsensors, which takes into account the combined effect of three processes: reversible adsorption, protein structural transformation, and depletion of the analyzed sample of protein molecules during adsorption. This is the first non-linear noise model that considers the random change of the biomolecule spatial structure, the effect that often follows the adsorption of proteins on a sensing surface. We use the developed model for the analysis of the effects that protein structural transformation and depletion of the analyzed sample have on the noise. The results of the analysis show their pronounced influence on the shape of the noise spectrum and on the noise power in the frequency range of interest, especially at low protein concentrations. The presented noise model and analysis are important for the estimation and optimization of sensing performance during sensor development, as well as for the development of highly sensitive measurement methods based on noise measurement.

Keywords: Biosensor, Protein Sensor, Sensor Noise, Mathematical Modeling, Adsorption, Protein Structure Transformation, Protein Conformation, Analyte Depletion.

Paper Id.: 99

Implementation of Multi-Bit error Detection and Correction Codes with Generator-Parity Check matrices

G. Shanthi[1], K. Srinivas Rao[2], Mohd Masood Hasan[1], H. Tanuja[1], Ch. Yashwanth[1]
[1] Department of Electronics and Communication Engineering VNRVJIET, Bachupally Hyderabad-500090, India
[2] Department of ECE, MEMS Research Center, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur 522502, India.

Abstract:

The numerous disruptions have an impact on how data is transmitted in complex space communications. Furthermore, these noises cause data burst errors. Low-density parity checking codes (LDPC) are therefore essential for locating and correcting errors. However, using the conventional hamming encoders and decoders, only one bit error was discovered and fixed. To identify and correct several bits of mistake, the Multi-Bit Error Detection and Repair Codes (MBE- DCC) are used in this work. An identity bit generator matrix and a parity bit generator matrix are used in the initial MBE-DCC encoding method. The damaged encoded data is then sent across the space communication link after being subjected to numerous interruptions and mistakes. Thus, At the receiver side the decoding procedure for MBE-DCC was carried out for space communications applications by making use of error location detection, syndrome detection, and error correction modules. The simulations revealed that the proposed MBE-DCC outperformed conventional LDPC methods.

Keywords: Error Detection and Correction Codes for multi bit data, encoding procedure, decoding procedure, syndrome decoding, error analysis, error correction modules.

Paper Id.: 52

The Role of Log Power Monitoring Channel of BTRR and Strengthening its Input Signal by Installing a Line Driver between NLW-1000 and PA-1000

Md. Bodhroddoza Shohag[1], Md. Sayed Hossain[1[0000-0003-4426-3956],*], Md. Rakibul Hasan[1], Md. Mobasher Ahmed[1], Abdullah Al Mahmud[1], Md. Moazzem Hossain[1], Mohammad Mezbah Uddin[1], Md. Abdul Malek Soner[1], Ashraful Haque[1], Nusrat Jahan[1] and Kamrul Alam Khan[2]
[1]Center for Research Reactor, Bangladesh Atomic Energy Commission, Dhaka, Bangladesh
[2]Department of Physics, Jagannath University, Dhaka, Bangladesh

Abstract

Various experiments require very low reactor power to full power and for low power experiments, Wide-Range Log Power Channel (NLW-1000) plays a solely vital role. Therefore, it should be operational during rector operation as well as shutdown state and without the proper functioning of NLW-1000, it will be impossible to observe reactor power in a logarithmic scale as well as rector period. Suddenly, the NLW-1000 was not working properly, therefore, a new NLW-1000 and pre-amplifier (PA-1000) were installed. Then, the prestart checks showed that the "count rate low test" and the "count rate high test" were failed and this information indicates that there is a signal loose between the PA-1000 and the NLW-1000. To cope with this issue, a line driver was installed in the data transmission line between NLW-1000 and PA-1000 but again the prestart check showed the same result as before. Then, an oscilloscope is used to know the signal condition at different points in the total transmission line and the continuity checks of STP showed that the optocouplers in the FC-ISO-D and FC-ISO-C were inactive. By making a proper connection, the problem is resolved. After the system powered up, the voltage outputs at each point of the FC-ISO-D and FC-ISO-C as well as the outputs of the oscilloscope at different positions showed normal conditions. After all, the total prestart checks of NLW-1000 were passed. Various types of experiments are now going on using this BTRR facility by observing reactor power in a logarithmic scale as well as rector period.

Keywords: Power Monitoring Channel; Line Driver; Research Reactor; I&C System; Signal Boosting.

Paper Id.: 57

Self-Recovered from SEU with High-Speed Radiation-Hardened (HSRH12T) SRAM cell for Space Application

Priyanka Sharma, Vaibhav Neema

Department of Electronics and Telecommunication,
IET-Devi Ahilya University, Indore, India

Abstract

Addressing the issue of Single Event Upset (SEU) in high-density SRAM designs is crucial to ensure reliable operation and data integrity. Researchers and engineers are continuously exploring various techniques and methodologies to mitigate the impact of charge sharing and reduce the occurrence of SEU-induced errors. By developing radiation-hardened SRAM designs and implementing strategies to minimize charge sharing effects, the reliability and performance of memory systems can be significantly improved. In this paper authors proposed high speed radiation harden (HSRH12T) SRAM cell design which is 100% recovery from Single event upset with the capability of recover from 5fC critical charge at space. The proposed cell exhibits high speed read and write operation, the cell has 56X higher read speed and 5.1X higher write ability as compare with mercenary competitor SRRD12T.The Monte Carlo simulation of 1000 points for read access time and write delay shows the stability of the proposed cell at 1 V Supply voltage.

Keywords: SRAM, SEU, Read Access Time, Write Delay, Critical charge.

Paper Id.: 69

Automation of Ultrafiltration Flow Control in Peritoneal Dialysis

[1]Zhilo N.M., [2]Guha K., [1] Pozhar K.V., [1] Putrya B.M., [1] Selishchev S.V. Department names

[1] Institute of Biomedical Systems, National Research University of Electronic Technology MIET, Moscow, Russia
[2]National Institute of Technology Silchar, Assam – 788010, India

Abstract

The paper proposes a method for control automation of the flow of excess fluid removal from the body during peritoneal dialysis, which consists in feedback control with predicting the volume of fluid in the peritoneal cavity. The key element of such a system is a noninvasive glucose meter based on infrared spectroscopy. The meter is based on a precision electronic current control circuit, as well as an optoelectronic pair operating in a pulsed mode, which registers changes in the absorbance of dialysate. A mathematical model has been developed for automatic calculation of the necessary corrective microboluses of glucose concentrate. Approbation of the system was carried out in the course of simulation tests, for which a mathematical model of a virtual patient was developed. During the simulation, it was shown that the proposed control method makes it possible to maintain the concentration of glucose in the dialysate with high accuracy, as well as to continuously provide the specified parameters for removing fluid from the body in the presence of a system for pumping excess fluid. The method is insensitive to errors in determining the parameters of the patient and to the variability of these parameters, as well as errors in the operation of the glucose meter, infusion pump and suction pumps. The developed system makes it possible to achieve high efficiency of ultrafiltration in peritoneal dialysis, reducing the procedure time for high-intensity dialysis, increasing the stability and physiology of fluid removal, as well as reducing the frequency of expendables replacement in continuous peritoneal dialysis.

Keywords: Ultrafiltration control, Automated peritoneal dialysis, Glucose monitoring, Feedback control.

Paper Id.: 83

A Proposed CMOS-based Design for Biologically Inspired LIF Spiking Neuron

Seenivasan M A, Adarsh V Parekkattil, Rekib Uddin Ahmed, Prabir Saha
Electronics and Communication Engineering National Institute of Technology Meghalaya – 793003, INDIA

Abstract

Neuromorphic computing has the potential to revolutionize autonomous systems and improve the energy efficiency of conventional computing systems, so it is recognized as the third generation of artificial intelligence (AI). The core part of the neuromorphic processors is called the spiking neural network (SNN) which is a more biologically plausible neuron model compared to ANN where the signal is propagated in the form of a spike. This perception seeks to create hardware systems that resemble the brain in both shape and function; these systems are comprised of artificial bio□neurons and synapses and can be scaled to the size of the brain. The various bio-plausible neuron models are developed by many researchers now to attain precise values of the neuron. This paper proposes a subthreshold implementation of the Leaky Integrate and Fire neuron model. Also, the proposed model is compared with popular models like Hodgkin-Huxley and Izhikevich models. The neuron models are simulated in the multi-sim simulator powered by National Instruments to understand the different spiking behaviors. The models comprise analog and mixed A/D circuits to mimic the biological spiking behaviors and exhibit bioelectric potential differences. The membrane potential changes generate the spike pulses with different shapes and magnitudes which have been indicated in this paper, to realize spiking behavior in the SNNs.

Keywords: Neuromorphic, Spiking, Bursting, bioelectric potentials, Hodgkin–Huxley, Izhikevich model, Integrate and Fire (IF), Leaky IF, Subthreshold, CMOS, Low power, Analog, mixed A/D circuits

Paper Id.: 85

VLSI Implementation of Convolution Chip: A Design Prospects

Harsh Raj Thakur, Seenivasn M A, Prabir Saha
Dept. of ECE National Institute of Technology Meghalaya, Shillong, Meghalaya, India

Abstract

In this paper, VLSI implementation of a decimal convolution algorithm has been implemented, through multipliers and adders which has been realized in parallel fashion to optimize the hardware burden. The concept uses parallelism at the algorithmic and architectural levels and parallel-adders and optimised multipliers have been utilized for convolution operations in hardware domain. The chip is designed to maximise performance while minimising power consumption, making it ap□propriate for environments with limited resources. Additionally, to improve the energy efficiency, low-power VLSI approaches including precision arithmetic operations and power management algorithms are also used. The proposed design has been simulated through Verilog coding for validating the results and synthesized in Vivado (xc7vx485tffg1157-1) for VLSI parameters estimation. This implementation result offers insightful information and promising future directions for designing energy-efficient VLSI solutions for discrete number-convolution algorithm.

Keyword: Multiplier, Adder, Convolution, VLSI, Arithmetic

Paper Id.: 90

Security of Data in MIMO Systems-An approach

Nabarun Chakraborty[1], Dipjyoti Narzari[2], Sabyasachi Bhattacharyya[3], Kandarpa Kumar Sarma[4]
Dept. of Electronics & Telecommunication Engineering[1,2,3,]
Dept. of Electronics & Communication Engineering[4]
Barak Valley Engineering College, Karimganj-788701, Assam[1,2,3], India
Gauhati University, Guwahati-781014, Assam[4], India

Abstract

Today's current communication systems are built in part on wireless technologies that employ increasingly compact and portable electronic equipment. This percentage is continually expanding. Consequently, the requirement to supply a lightweight data is increasing and hence the need for a security plan for these systems is getting worse. This paper focuses on two methods from the Physical Layer Security (PLS) field, which is an active area of study. The fundamental PLS techniques have been around for a while, but further research is needed to see whether they offer any potential secrecy advantages. With the advancement of Multiple Input Multiple Output (MIMO) multi-antenna systems, interest in these possible benefits has grown.[1] The first PLS method in this paper, that is taken into consideration is beamforming, which is made feasible by MIMO. Here, a sender can route the information signal in the intended receiver's direction while lowering the signal quality seen by a possible spy. The practice of artificial noise (AN), in addition to beamforming, is researched. In order to further hinder an eavesdropper's capacity to identify and decode the information signal being delivered to the intended recipient, AN mandate that the sender produce a random noise signal in addition to the information signal. These PLS approaches are used in MATLAB simulations, and the outcomes are given.

Keywords: Physical Layer Security, Beamforming Artificial Noise, Maximal Ratio Combining, Multiple Output Multiple Input, Multiple Input Single Output, Zer Forcing.

Paper Id.: 93

Design and Analysis of RF MEMS Series Switch with high Isolation

Y. Anusha[1], Koushik Guha[2], M. Kavi Charan[3], K. Srinivasa Rao[4]
[1]Research Scholar, Department of Electronics and Communication Engineering, MEMS Design Center, National Institute of Technology, Silchar, Assam 788010, India.
[2,3]Department of Electronics and Communication Engineering, MEMS Design Center, National Institute of Technology, Silchar, Assam 788010, India.
[4]Microelectronics & VLSI Research Group is a research group affiliated with the Department of Electronics and Communication Engineering at Koneru Lakshmaiah Education Foundation (KLEF). KLEF is a deemed-to-be-university located in Vaddeswaram, Andhra Pradesh, India.

Abstract

In this paper, we have focused on the design, simulation, and analysis of an RF MEMS series switch with a high isolation. The proposed RF MEMS switch has been designed and simulated using Finite Element Method (FEM) tools, which enable detailed analysis of its mechanical and electrical performance. Through optimization, they have determined that the optimized beam thickness of the switch results in an actuation voltage of 1.6 V for a 0.5 μm beam thickness, while the actuation voltage calculated using the mechanical model is 2.1 V. The simulation results of the proposed RF MEMS switch exhibit favorable S-parameters, including a return loss of 15 dB and an insertion loss of 0.027 dB. Additionally, the switch demonstrates a high level of isolation, with a measured value of -72 dB at 70 GHz. Overall, the simulation results align closely with the calculated values, indicating the reliability and accuracy of the proposed design. The switch not only achieves a low actuation voltage but also offers a compact size, making it promising for applications requiring efficient RF performance.

Keywords: RF MEMS Series Switch, Actuation Voltage, Ligament Efficiency, Parallel Plate Capacitance, Insertion loss, return loss, Isolation.

Paper Id – 103

Read/Write Improved Low Leakage 10 T SRAM Cell for Battery Operated Biomedical Applications

Ashish Panchal, Nidhi Tiwari, Vaibhav Neema
Electronics and Communication
SAGE University, Indore – 452001, INDIA
IET-Devi Ahilya University, Indore – 452001, INDIA

Abstract

Advancements in healthcare have been made possible through the development of portable biomedical devices that provide convenient and effective solutions for diagnostics and monitoring. These devices heavily rely on memory cells to accurately store and process biomedical data. To facilitate this process, biomedical signals need to be shared and processed between the cache and processor. However, integrating memory cells into portable biomedical devices comes with its own set of challenges, including limited power sources, size and weight limitations, and the need for reliable performance even in noisy environments. To overcome these challenges, this paper introduces a new memory cell design called 10T SRAM, specifically tailored for biomedical applications. In order to evaluate its performance, we will examine several factors, such as stability, speed, power consumption, and voltage requirements. The proposed 10 SRAM Cell is 1.15X more stable than the BT8T and 9T SRAM cells; it accessed data 1.3X faster than the BT8T SRAM cell; and it has 50% less leakage power than the BT8T SRAM cell. These findings are important because they contribute to the development of cache memory, specifically for biomedical applications. This paper is an important step towards solving memory-related challenges in the biomedical field and opens up possibilities for further advancements in this area.

Keywords: Portable biomedical devices, SRAM memory cells, stability, low power, write ability, reliability, and power efficiency.

Paper Id – 103

Low Power 7T SRAM Cell Design with Reduced Leakage Power

M. Damodhar Rao[1 *], Y. V. Narayana [2], V.V.K.D.V. Prasad [3]
[1*] Research scholar, JNTUK, Kakinada, AP, India.
[2] Professor, Department of ECE, Tirumala Engineering College, Narsarao pet, Guntur, AP, India.
[3] Professor, Department of ECE, Gudlavalleru Engineering College, Gudlavalleru, Krishna, AP, India.

Abstract

Static Random Access Memory (SRAM) plays vital role in modern digital systems design. However, scaling down the SRAM cell size to achieve higher integration densities has led to several challenges, including reduced stability margins, increased power consumption, and susceptibility to process variations. In this work, a novel 7T SRAM cell architecture is proposed that to addresses these issues by improving the stability margins, reducing power consumption, and enhancing the tolerance to process variations. 7T SRAM cell utilizes NMOS and PMOS transistors in combination and a feedback loop to maintain the cell's stability during the operations of read and write. The proposed cell has been simulated using 45nm CMOS technology, and the results show a significant enhancement in stability gap compared to a standard 6T SRAM cell. This cell consumes little power. Furthermore, the 7T SRAM cell demonstrates better performance in the presence of system variations, making it a promising candidate for future high-density memory applications.

Keywords: SRAM cell, SNM, Power dissipation, CMOS.

Innovative Education in Pleasant Environment

Dulal Acharjee

Director, Applied Computer Technology, Kolkata, WB, India.
Email: dulal@actsoft.org

Abstract: This writing presents some concepts of innovation and invention, discusses old inventions and recent inventions. Discussions are guided towards- how an invention can be converted to industry product and can attract more people to do more businesses.

Invention and innovation: Anything new are called inventions. Continuous improvements over invention is known as innovations. It is the advancement over existing process or object. Innovative education teaches the process of delivering the teaching materials aiming that it will grow the thinking pattern of students to innovate the system which finally target to make an invention. Alternatively, it will teach how to grow desire or appetite of creating of something new.

Different types of innovation: as per OECD's (Organisation for Economic Co-operation and Development) Descriptions), there are four types of innovations as:

(i) *Product Innovation:* it is called developing a new machine ever seen before. as example wireless machine invention (1895), steam engine (1712) by Thomas Newcomen, airplane (1903) by Wright brothers etc.

(ii) *Process innovation:* these are managerial manual processes, computer processes, algorithms etc. As example: Life cycle of any production phases, Six Sigma steps, data sorting algorithms, data security encryption-decryption processes, testing phases of a medicine etc.

(iii) *Marketing Innovation:* as per IBM's process analysis, there are three areas of innovations in marketing and these are: * Resource allocation, *Revenue planning and *Campaign optimization. (for more study: 'The Market', Matthew Watson).

(iv) *Organizational Innovation:* it comprises innovation-culture, innovation-capability, continuous improvements, process improvements etc. These are mostly related with business organization's capability growth for innovations. Study and following of standard processes through practical observation can grow capabilities of innovations.

Examples of inventions: Invention is the new creation which should be proved by experiments, logically or theoretically or through implementations in social lives. It is the rule of justification-evolution-verification of invention. In arts and culture, invention can't be proved by experimentally. But, effects of theory can be metered through study of pre and post data collected from that area. Some examples of old inventions:

(a) *Example of Science-invention:* In 1895, Jagadish Chandra Bose invented wireless signal and ringed a bell to a far distance of 75 ft. That was the first-time demonstration of wireless communication. Figure of that instrument is shown below:

Fig-1: instruments used for transmission of electro-magnetic signal. Image source: Wikimedia

(b) *Example of Cultural innovation:* Models of Dinosaurs: in 1993, Jurassic Park film is Directed by Steven Spielberg and it was too famous due to different models of Dinosaurs. Due to this innovative application of models of Dinosaurs, next time, most of the children parks had become attractive with these animated models with sound and movements.

Fig-2: models of Dinosaurs in Jurassic Park. Source: alamy.com

(c) *Example of Historical innovation:* Darwin's(1809–1882) 'On the Origin of Species'(1859) explained the theory of evolution of life and described that, for a long time of evolution over reproduction and natural selection, the final species(homo sapience) as human is evolved. This is an example of Darwin's evolution of species of living animals and trees. It is known as philosophical, geographical and historical evolution.

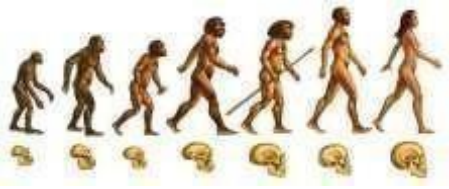


Fig-3: evolution of human. Source: https://byjus.com/

Modern inventions: some examples of recent inventions in science and engineering:- Fuzzy Logic, data sorting algorithm, encryption-decryption, Blue LED (Light Emitting Diode), Corona vaccine are important, micro-nano Processors etc. Below in fig-4, it is shown the uses of Fuzzy logic in a washing machine as a button of 'Fuzzy'. Machines have become intelligent to make decision as when to move the motor speedy, slow or speedier etc. Prof. Lotfi A Zadeh (1921-2017), a professor of electrical engineering, invented computational methods of Fuzzy Logic (in between 0 and 1 there may be many inputs and output levels) and after that most of the electronic machine manufacturers used that theory within the machine for making intelligent decision for the undefined situations. Below, a front panel of a washing machine is shown where a 'Fuzzy' button is marked by red arrow by the author.

Fig-4: Fuzzy button of a washing machine

Developing desires of invention: this is the major teaching art that how to grow sense of innovation or desire of invention of something within the members of the group. If the history of any invention is studied it is found that there is a long step by step achievements. Solution of any problem has many steps and students-learners should have that patience to solve the last step of the solution. As example, finding a general equation or formula for calculating next elementary number in number system is not yet solved. There is no formula to compute elementary number series. Yet, the World research people could not invent it. Any invention has a pleasure and satisfaction of mind.

How a teacher can give an approach of innovation/invention to the learners: as an example, say, irrigation is a common problem: present solutions are: water pump, canal water, reserving water in pond, storing rain water etc. then students may write about what are other solutions? If a new concept comes that may be considered as an innovative idea.

Comparisons of invention, innovation, and reform:

Invention	Innovation	Reform
Something creating newly	Improvement of previous invention.	Break and build without innovation
New creation as seen ever	Successive progress on existing work	Changing gesture and posture with new flavor.
Creating new which has scope of developing next versions	New and newer version of previous invention	Inner product is same, only outer label is changed by new name.

Stages of innovation: requirements of each stage are that innovation gives a better solution of each of the steps of the problem; maybe, in future in next stage best solutions may come. As example, a touch screen is a better solution of the input of data than previous input devices as mouse, keypad etc.

Environment of innovation: A good environment can give a better output. For different subject different environment is required. For example, a coal furnace of old railway engine needs quality furnace to hold sufficient heat else some heat will be lost. So, for better output, environment is a matter. Home environment is most important, if parents can show their success to children with patience, some better innovative desires will grow within the children. Group learning, team work can dissipate knowledge within the team is a short time which may not be possible long reading from the book.

Effects of pleasant environments: if health and mind can synchronize with each other, output performed by the person would be better while other parameters remain same. Games are essential for the both teachers and

students. Modern learning tools like: electronic toys, manual tools of educations like- Globe, light ball, Laser pen, Video games etc. has different levels of learning aspects as assemble, operation, manufacturing, components behavior, inside composition etc. To make the learning environment more pleasant, developing Toy's laboratory in school-colleges can grow knowledge of manufacturing also students' satisfaction can be increased. An example of pleasant play-ground of minor students are shown:

Fig-5: a play ground as a pleasant environment. Source: Linkedin.com, page of Geeta Verma.

Conclusion: there is no short cut path of learning. Some better practices may help to accelerate the system. Here, some issues are described to understand invention and innovative approaches. Invention makes the machine and the environment more user friendly and adaptable which has made the World comfortable and pleasant. Last words are- help others to think about invention-innovative methods and apply those concepts in a pleasant environment.

References:

https://www.researchgate.net/post/How_could_we_create_an_innovative_learning_environment
https://www.researchgate.net/publication/352569560_Innovation_in_Education
https://www.oecd.org/education/ceri/GEIS2016-Background-document.pdf
Cerna, L. (2014), "Innovation, governance and reform in education", CERI Conference background paper, 3-5 November 2014, *www.oecd.org/edu/ceri/CERI%20Conference%20Background%20Paper_formatted.pdf*.
Hikmet, N., Taylor, E., & Davis, C. (2008). ―*The* S*tudent Productivity Paradox*: *Technology Mediated Learning* in *Schools*. Communications of the ACM, 51(9), 128-131.

Micro2023, 01st – 03rd July, 2023.
Venue: Hotel Vivanta, Guwahati, Assam, India.
Organizer: Applied Computer Technology, Kolkata, India
List of invited Speakers/ Session Chairs

	Keynote Speaker: **Prof. Sergei Selishchev,** Director, Institute of Biomedical Systems, National Research University of Electronic Technology, Moscow, Russia. Talk Title: Digital twin of implantable total artificial kidney with reabsorption and ultrafiltration imitations: a puzzle
	Keynote Speaker: **Dr. Jacopo Iannacci,** Centre for Materials and Microsystems (CMM), Fondazione Bruno Kessler (FBK), Trento, Italy.
	Invited Speaker: **Prof. Abhijit Biswas** Professor & HOD, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2023).
	Invited Speaker **Dr. Srinivas Rao** General Chair of Micro2023, and Professor, Department of ECE, K L University, Guntur, Andhra Pradesh.
	Invited Speaker **Dr. Shweta Gupta** Department of ECE, Jain University, Bengaluru, Karnataka, India.
	Keynote Speaker **Dr. Massimo Donelli,** Canter for Security and Crime Sciences, University of Trento and Verona, Italy.
	**Dr. Moumita Mukherjee** Dean (R & D), Adamas University, Barasat, Kolkata, West Bengal, India. (Ex. Sr. Scientist of DRDO Centre of Excellence) (under Ministry of Defence, Govt. of India).

	Invited Speaker **Dr. Koushik Guha** Associate Dean (Academics), National Institute of Technology, Silchar, Assam, India.
	**Dr. Sandip Chanda** Associate Professor and Head of Electrical Engineering Department Dean Faculty Welfare Ghani Khan Choudhury Institute of Engineering and Technology
	**Dr. Prabir Saha** Dept of ECE, National Institute of Technology, Meghalaya
	Prof. (Dr.) Kandarpa Kumar Sarma Professor & HOD, ECE, Gauhati University, Assam.
	**Prof. (Dr.) Jibitesh Mishra** Odisha University of Technology and Research, Bhubaneswar, Odisha.

Advertisement:

CCSN2023

12th International Conference on
Computing, Communication and Sensor Networks

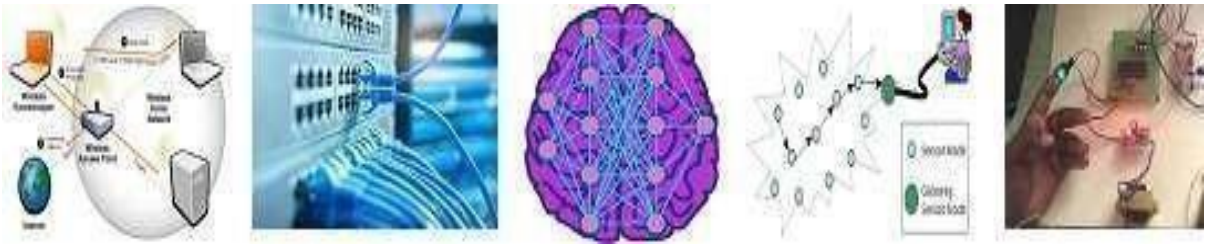
(Physical mode / Online mode Conference)

Venue: Mumbi, Maharashtra, India,

Website: actsoft.org/ccsn2023

Conference date: 14th to 16th October, 2023

Organizer: Applied Computer Technologies, Kolkata, WB.



Contacts:

1. **Dr. Punyaban Patel,** Professor, Department of CSE, CMR Technical Campus, Hyderabad, India. Email: punyaban@gmail.com

2. **Dr. Abhishek Das,** Associate Professor, CSE, Aliah University, New Town, Kolkata, West Bengal, Email: adas.us@gmail.com

3. **Prof. D Acharjee**, Executive Chairman, ESDA2023, and Director, Applied Computer Technology, Kolkata, India. Email: esda.conference@gmail.com, info@actsoft.org

Advertisement:

ESDA-2023

6th International Conference on

Energy Systems, Drives and Automations

(Physical mode / Online mode Conference)

Venue: Kolkata, West Bengal, India,

Website: www.actsoft/esda2023

Conference date: 30th and 31st of December, 2023

Organizer: Applied Computer Technologies, Kolkata, WB.



Contacts:

1. **Prof. Pradip Kumar Sadhu,** Department of Electrical Engineering, IIT(ISM), Dhanbad, Jharkhand.

2. **Dr. Sandip Chanda,** Associate Professor Department of EE, Ghani Khan Choudhury Institute of Engineering, West Bengal, India. Email: sandipee1978@gmail.com

3. **Prof. D Acharjee,** Executive Chairman, ESDA2023, and Director, Applied Computer Technology, Kolkata, India. Email: esda.conference@gmail.com, info@actsoft.org

Abstract Proceeding Book: Micro2023

Board of Editors: